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INVESTIGATIONS OF GATE TURN-OFF STRUCTURES

New Jersey Institute of Technology D.ENG.SC. 1981

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INVESTIGATIONS OF
GATE TURN-OFF STRUCTURES

by

Hans Werner Becke

Dissertation submitted to the Faculty of the Graduate School of the New Jersey Institute of Technology in partial fulfillment of the requirement for the degree of

Doctor of Engineering Science

1981

APPROVAL SHEET

Title of Thesis: Investigation of Gate Turn-Off Structures

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Mr. Becke holds a B.S. degree in EE from the Ohm-Polytechnical Institute, Nuremberg, Germany (1953). He received the MSEE degree from New Jersey Institute of Technology (1966) and has completed his dissertation for a D.Eng.Sc. in Electrical Engineering at the same institute (1981).

Mr. Becke has over 20 years of experience in the semiconductor field. The major portion of his career he spent with RCA Corp. From 1961 to 1967 he worked mainly on GaAs devices, such as bipolar power transistors, IR diodes and semiconductor lasers. He is credited with the development of the first GaAs insulated gate-field effect transistor.

From 1967 on, Mr. Becke was engaged in development of silicon technology for high power transistor structures and dielectrically isolated IC's. Noteworthy are his contributions in the area of gate turn-off thyristors directed toward achievement of safe turn-off and high performance, and in the development of power MOS FETS.

In 1980, Mr. Becke joined the High Voltage IC Department of Bell Labs, where he is currently designing high voltage dielectrically isolated devices.

Mr. Becke holds 11 patents and has published 16 papers dealing with semiconductor topics[1].

[1] A list of Publications and Patents is included at the end of this thesis, following the bibliography.

ABSTRACT

Research and Development was done on gate turn-off devices. The aim was i) to improve turn-off capability without compromise of turn-on, on-state, and useful temperature range, ii) to implement "safe" turn-off.

A) The dependence of the electrical device characteristics on cathode width for an optimized vertical structure was determined. Fall times of 100 to 200 nsec and risetimes of <400 nsec were simultaneously obtained for average current densities of 53 A/cm^2 @ T_j = 125°C. From spreading resistance analysis the fast t_r and t_f response is shown to be a consequence of proper Au-distribution in the active device volume.

From transient analysis it is concluded that for safe turn-off d^2i_A/dt^2 should never become positive during the fall phase, and that the differential turn-off gain should remain less than unity during the tail period. These requirements are realized by means of a voltage source with a series inductance as gate input for turn-off. As a result

a switching capability of 1.56kW (resistive load) @ 75°C case temperature at 50kHz and with 97% device efficiency is obtained for a chip of $0.15cm^2$.

B) Anode shorts for improvement of turn-off without the necessity of excessive lifetime reduction were also investigated. These shorts substantially reduce the turn-on sensitivity.

A Schottky barrier in series with the non-regenerative region, which parallels the thyristor section, restored the turn-on sensitivity at low temperatures while retaining the turn-off capability at high temperatures.

For 30A ($\overline{J}$ = 200 A/cm^2) turn-off @ +125°C the gate trigger current was ∿10mA and 60mA @ -40°C for devices with Schottky barriers and without Schottky barriers, respectively.

C. The incidence of catastrophic failures due to filamentary burn-out was drastically reduced through introduction of a dynamic ballasting (defocusing) concept. This approach features a resistively ballasted cathode (∿7Ω/square) with an insulated

center, i.e., contacted only at the periphery.

Therefore, the formation of small area, high current density filaments is largely inhibited. Using this principle, device operation was extended from -20°C to +125°C for conventional devices, to a range from -60°C for sensitive turn-on (I_{gt} = 300μA) to +150°C for safe turn-off @ $I_{T\ off(max)}$ = 8.5A (J = 55A/cm^2) for the ballasted devices.

PREFACE

The search for efficient electronic power switches has gained more and more importance during the last decade. Energy shortage and inflation have made it necessary to look for new technological solutions to provide devices for power conversion equipment that will be both more efficient and at the same time economical.

The Gate-Turn-Off thyristor, though known conceptionally since the early 60's, has in the past eluded attempts to make it a practical reality as a viable, useful electronic component.

The experimental work, subject of this thesis, was directed toward identification of the problems with this device, and to gain a better understanding, at least qualitatively, of the turn-off process.

Hopefully, the new concepts introduced to improve device performance have contributed toward advancement of the state-of-the-art. The results, especially those obtained by the application of a Schottky barrier in series with anode shorts and the implementation of the dynamic ballasting principle, are very encouraging. They should provide an incentive for further investigations of GTO-structures and eventually lead to a complete understanding of phenomena related to this device, such that from a theoretical basis device performance and limitations can be predicted.

I appreciate the help provided by Professor R. P. Misra of NJIT as my Thesis Advisor. I am also greatly indebted to Dr. M. H. Zambuto for the help and encouragement received over the years of my graduate studies, the doctoral program. My thanks also to Dr. K. S. Sohn and Dr. M. Natapoff for taking the time to critically read this dissertation.

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I acknowledge the great value of discussions related to this work I had with many of my colleagues, especially to Messrs. J. M. Neilson, K. P. Smith, R. Amantea, and R. Martinelli I extend my gratitude.

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Last but not least, I thank Mrs. R. Lepree for the fast and flawless typing of this manuscript.

To Friedl and Hans-Dieter

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LIST OF SYMBOLS

Symbol	Description	Page of First Appearance
α_1	Common base current gain of transistor 1, (NPN)	4
α_2	Common base current gain of transistor 2, (PNP)	4
β_1	Common emitter current gain of transistor 1, (NPN)	4
β_2	Common emitter current gain of transistor 2, (PNP)	4
D_n	Diffusion coefficient	19
$E_{A(t_{f1})}$	Anode energy absorbed during fall time t_{f1}	97
$E_{A(t_{f2})}$	Anode energy absorbed during tail period t_{f2}	97
$E_{A(tr)}$	Anode energy absorbed during rise time interval	97
$E_{D(tot)}$	(Total) Absorbed energy per cycle	96
$E_{G(t_{f1})}$	Gate energy absorbed during fall time t_{f1}	97
$E_{G(t_{f2})}$	Gate energy absorbed during tail period t_{f2}	97
$E_{G(tr)}$	Gate energy absorbed during rise time interval	97
$E_{(on)}$	"On" state energy	97
$E_{t(off)}$	(Total) Turn-off energy absorbed	97
$E_{t(on)}$	(Total) Turn-on energy absorbed	97
f	Frequency	98
F_D	Duty factor	96

Symbol	Description	Page of First Appearance
G_{gq}	Turn-off gain	6
$G_{gq(max)}$	Maximum turn-off gain	24
G_L	Loop gain	5
h_{FE}	DC-current gain (common emitter)	66
Θ	Thermal resistance	98
I_A	Anode Current	4
$I_{A(max)}$, $I_{T\ off(max)}$	Maximum anode current that can be turned off	27
I_G	Gate current	4
I_{gt}	Gate trigger current	50, 61
I_{gq}	Gate current during turn-off	66
I_k	Cathode Current	15
I_T	"On" state current (forward conduction current)	50, 82
I_z	z-component of current	20
J_1	Gate-cathode junction	16
J_2	Center (forward blocking) junction	16
J_3	Anode (reverse blocking) junction	16
J_z	z-component of current density	19
$J_{z(max)}$	Maximum Current Density	21
$J_{z(on)}$	(Average) On-state current density	21

Symbol	Description	Page of First Appearance
L_{gs}	Gate Series Inductance	68
L_n	Diffusion Length (minority carriers)	19
L_x	Cathode Width	18
L_y	Cathode Length	16
N, n	Donor (electron) dominated semiconductor region	4
N^-, n^-	Lightly doped N region	8 ,17
N^+, n^+	Heavily doped N region	8, 17
$\|N_A\|$	(Absolute) acceptor concentration	47
$\|N_D\|$	(Absolute) donor concentration	47
n_e	Electron concentration	18
P, p	Acceptor (hole) dominated semiconductor region	4
P^-, p^-	Lightly doped P region	8, 17
P^+, p^+	Heavily doped P region	8, 17
P_D	Power dissipation	99
q	Electron charge	19
ΔQ	Charge in Δx_b	22
Q_N [1]	Charge in Base	29
Q_{off}	Total charge in device volume during turn-off	11
R_g	Lateral gate resistance	25

[1] For definition of symbols in Pg. 29-40 Kurata's notation is strictly followed. Please turn to the defining Figures 2-6 and 2-10.

Symbol	Description	Page of First Appearance
R_G	Gate series resistance	15
R_i	Internal device resistance	14
R_L	Load resistance	14
R_{sp}, $R_{\square p}$	Gate (p-base) sheet resistance	48 ,51
$\overline{\rho}_p$	Average gate (P-base) resistivity	25
t	Time	22
T	Temperature	50
t_1	Time instant at initiation of turn-off	11
t_2	Time instant at completed turn-off (Q = 0)	11
t_d	Delay time	--
t_f	Fall time	15
t_{f1}	(Forced) Fall time to tail break	96
t_{f2}	Tail decay time constant	96
T_j	Junction temperature	98
t_{off}	(Total) Turn-off time	119
t_{on}	(Total) Turn-on time	64
τ_{pA}	Hole life time in vicinity of anode	97
t_p	P-base (Gate) transit time	48
$t_{p(off)}$	Duration of turn-off pulse	96
$t_{p(on)}$	Duration of turn-on pulse	96
t_r	Rise time	50 ,51
t_s	Storage time	15

Symbol	Description	Page of First Appearance
T	Duration of period	96
τ_B [1]	Minority carrier lifetime in base (Gate)	29
τ_{eff}	Effective lifetime	19
τ_n	(Average) lifetime in N-base	50 ,51
$\overline{\tau}_p$	(Average) lifetime in P-base (gate)	73
V_A	Anode Voltage	14
V_D	Anode supply voltage	50, 68
V_{DRXM}	(Maximum) forward blocking voltage with parallel gate-cathode resistor	61
$V_{G\ br}$, V_{Gk}	Gate-Cathode breakdown voltage	8
V_{goc}	Gate source voltage	68
v_s	Spreading velocity	66
V_T	On-state voltage (across anode-cathode), forward voltage drop	51
W_p	(Gated) P-base width	16
x_{j1}	Cathode-gate junction depth coordinate	47
x_{j2}	Center (forward blocking) junction depth coordinate	47
x_{j3}	Anode (reverse blocking) junction depth coordinate	47
x_b	Transition coordinate (moving boundary during turn-off)	16
Δx_b	Transition region from "On" state to "Off" state	16

I. INTRODUCTION

A. Thyristors and Transistors as Electronic Switches

Four layer semiconductor structures (i.e., NPNP or PNPN), generically known as thyristors, exhibit characteristics similar to those of gas thyratrons. They may be triggered from a high voltage blocking state ("off") into a high current state ("on") by means of a single pulse applied to the control electrode, the gate. Thus, we could consider this semiconductor structure the electronic switch analogous of the electro-mechanical, latching relay.

Once the four layer device is in the "on" state, it is self regenerative, and turn-off may be achieved only if the anode voltage is removed for a time, sufficiently long to cause the decay of conduction current below the "holding" level.

We may now compare the features for electronic switching of a transistor with those of a thyristor.

Transistors can be switched from the control electrode (base) into the "on" state with considerable power gain. For example: the drive power may be 1.5 watts, derived from a 50% duty cycle square wave input of 1.5 volts and 2.0 amperes. The load power may be 750 watts for a current of 10 amperes through a resistive load with a 150 volt supply voltage. Thus the power gain is 500. The drive power has to be supplied to the base during the entire "on" time. Turn-off (without regard to speed) is accomplished by simple interruption of the drive circuit.

Thyristors can be switched from the gate with even higher power gain, because the trigger current may be kept in the milliampere range and the output current is limited essentially by the load resistance. For example: The input energy for triggering may be 150×10^{-9} watt-seconds for a 1 milliampere, 1.5 volt input pulse lasting 100 microseconds. The load power may be 750 watts for a current of 10 amperes through a resistive load, switched at a rate of 1.0 kilohertz with 50% duty cycle from a 150 volt supply. Thus, the power gain is 1×10^{7}, indeed very high.

A drive pulse is not required during the "on" time. Turn-off is accomplished by interruption of the load current, i.e., by means of commutation of this current through passive and active components of similar ratings than those specified for the actual power switch. Therefore, a considerable turn-off effort is required.

As we can see, the transistor is good for turn-on and poor for the "on" state when used as an electronic switch, while the thyristor is excellent for the "on" state and poor for turn-off, considering the same class of applications. Generally, transistors are more suitable for lower power and higher frequency operation, whereas thyristors are better employed when higher power output and lower frequency is called for.

B. The Gate Turn-Off Thyristor (GTO)

A desirable technical solution to an electronic switch would be, to have a device which combines the high frequency and/or high power capabilities of both transistors and thyristors, respectively, which can be switched "on" and "off" from the control electrode with a high power gain, and in addition does not need external drive power in order to remain in the "on" state.

Indeed, examination of the physics for four-layer structures and application of transistor theory indicates, that the realization of such a switch is possible. This switch is known as a Gate Turn-Off thyristor (GTO).

A device with turn-off capability from the gate was first described by J. M. Goldey, et al.[60-1] and R. H. vanLigten, et al.[60-2]

The important points of the existing theory for GTO's will be presented in chapter II. However, some general, qualitative statements concerning the possibility of turn-off from the gate and the difficulties encountered are given here.

1. Simple, First Order Observations

The four layer structure of Figure 1-1a may be considered as a composite of an NPN and a PNP structure interconnected as shown in Figure 1-1b. Thus, a two-transistor equivalent circuit can be constructed containing a complementary transistor pair in a feedback configuration as shown in Figure 1-1c. From the currents and gain

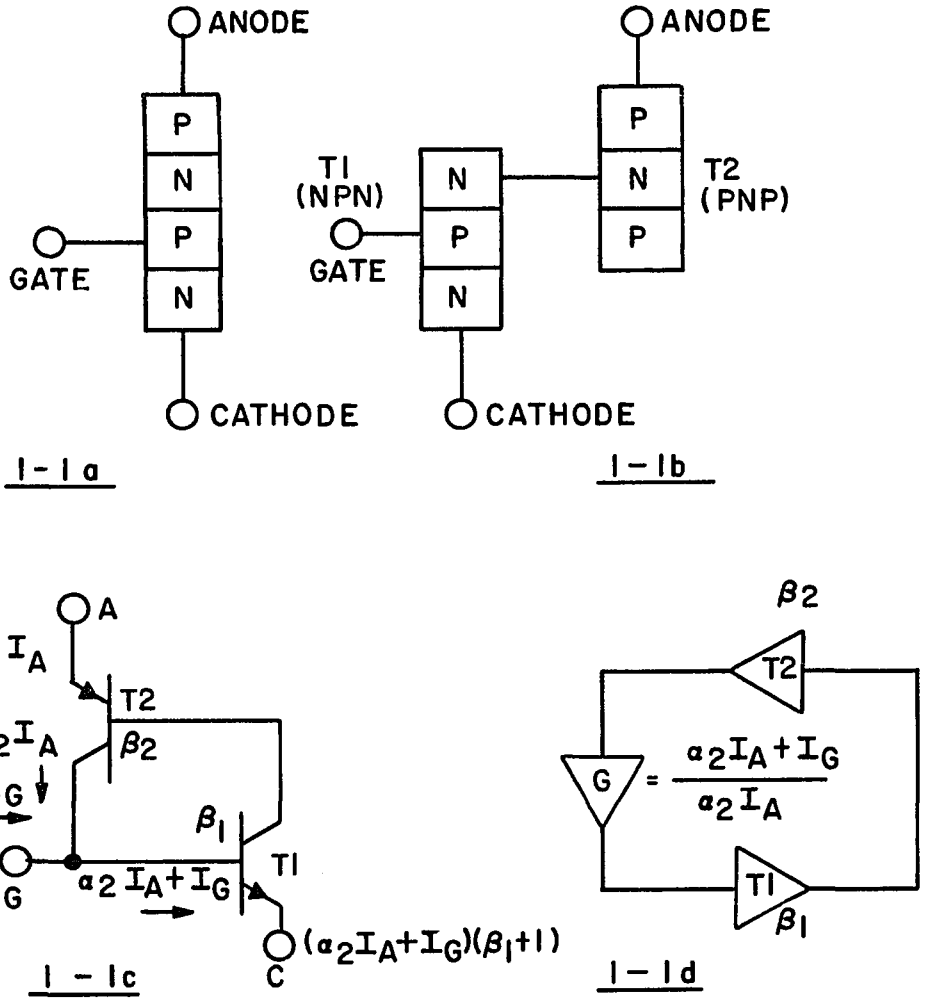

Figure 1-1. GTO Thyristor

Figure 1-1a. Schematic Four Layer Structure

Figure 1-1b. Composite NPN-PNP Structure

Figure 1-1c. Equivalent Transistor Circuit

Figure 1-1d. Loop Gain Diagram

factors in this figure, we may show in Figure 1-1d the loop gain with the gate terminal included. From these, we obtain the following:

$$G_L = \beta_1 \beta_2 \frac{\alpha_2 I_A + I_G}{\alpha_2 I_A} \qquad 1\text{-}1$$

where: G_L = total loop gain,

β_1 = common emitter current gain of transistor T_1

β_2 = common emitter current gain of transistor T_2

α_1 = common base current gain of the transistor T_1

α_2 = common base current gain of the transistor T_2

I_A = anode current, and

I_G = gate current

The condition for "turn-on" is given when the value of the loop gain reaches unity. Thus, the device will switch into the conducting state at

$$G_L = \beta_1 \beta_2 \frac{\alpha_2 I_A + I_G}{\alpha_2 I_A} \geq 1 \qquad 1\text{-}2$$

Since the gain for any transistor initially increases with current to a peak value, once the product $\beta_1 \beta_2$ becomes unity, the device will remain "on" without a gate signal.

It is now apparent that the condition for "turn-off" is reached, if it is possible to reduce the loop gain by some means again to a value equal or less to unity. This can be accomplished by reversal of the gate current. Thus, for turn-off, the relation 1-2 for the loop

gain G_L changes to

$$G_L = \beta_1 \beta_2 \frac{\alpha_2 I_A - I_G}{\alpha_2 I_A} \leq 1 \qquad 1\text{-}3$$

We may now define a "turn-off gain" as the ratio of anode current in the "on" condition to the gate current necessary to reduce the loop gain to unity. Using equation 1-3 and the relation $\alpha = \beta/(\beta + 1)$ we get

$$\frac{I_A}{I_{G/G_L=1}} = G_{gq} = \frac{\alpha_1}{(\alpha_1 + \alpha_2) - 1} \qquad 1\text{-}4$$

Equation 1-4 gives some qualitative guidance for the choice of the α's. It can be seen that a high turn-off gain may be obtained for α_1 being close to unity if α_2 is kept small (i.e., $\sim$0.2) at the same time. However, above discussion is only useful for explaining the basic concept of obtaining turn-off in an NPNP structure. Specifically, we have to take notice of the fact that any practical device is three dimensional, and variations in at least two dimensions have to be considered.

2. Qualitative, Two-Dimensional Considerations

The dynamic behavior of a two-dimensional model is described by E. D. Wolley[66-1] in which he finds a relationship between turn-off gain and turn-off time under the assumption of a constant gate current during the turn-off phase. M. Kurata[74-1] developed this two dimensional approach further using the charge control concept.[57-1] This

CAD model assumes that in the expression for the (one dimensional) turn-off gain the α's are constant.

In an actual device, however, the α's are functions of current density, temperature, anode voltage, and spatial distribution, and a constant gate current can only be approximated. Furthermore, the turn-off process involves a continuously changing current distribution within the device. Thus, when considered from this point of view, the α's become functions of time. Therefore, Equation 1-4 does not provide sufficient insight into the turn-off mechanism of a GTO.

In general, during the turn-off process the conducting electron hole plasma is deflected from an area close to the gate having the highest negative potential to the most remote area beneath the cathode with the least negative potential. Figure 1-2 illustrates this fact. In Figure 1-2a, we see the device in its "on-state" condition, conducting uniformly over the entire cathode area. Upon application of a negative bias to the gate, the plasma is "squeezed"[66-1, 74-1] into a high current density filament as shown in Figure 1-2b. Resultant local heating will often cause hot spots and thus device failure. This phenomenon is similar to reverse second breakdown in transistors,[67-1, 71-1] but generally more severe; because of the regenerative nature of this device, the current is restricted only by the external load resistance. Moreover, the negative gate current flowing through the lateral base resistance during turn-

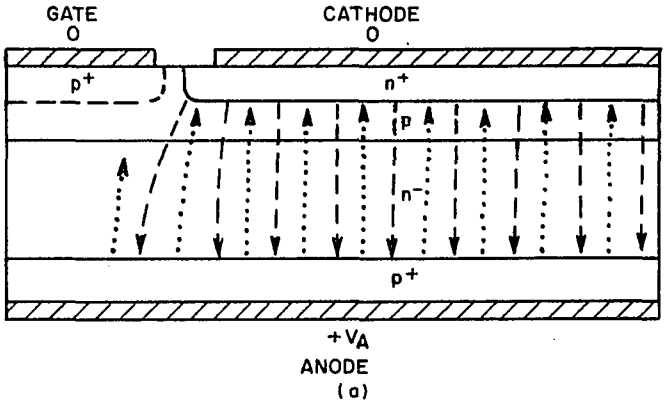

Figure 1-2a. GTO-Thyristor in "On" State

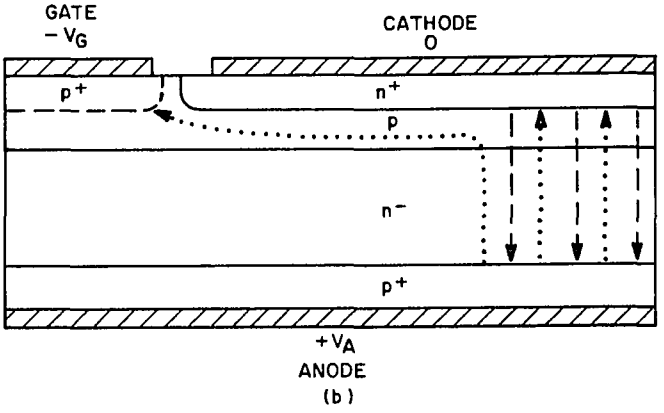

Figure 1-2b. GTO-Thyristor during Turn-Off

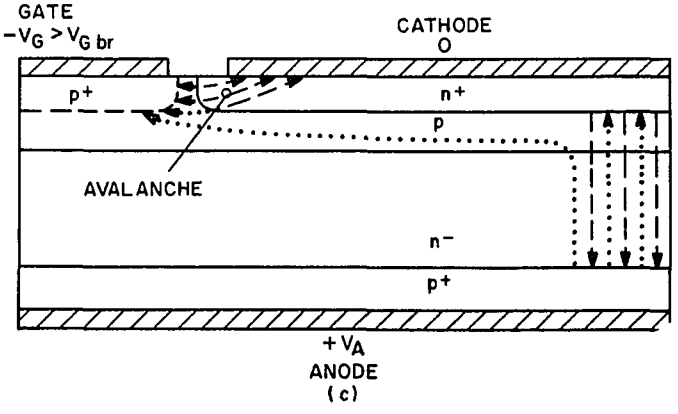

Figure 1-2c. Lateral Voltage Drop—$V_G > V_{G\,br}$

Figure 1-2. Turn-Off Process in Conventional GTO-Thyristor

off will produce a voltage drop which may reach the gate-cathode breakdown voltage at a current smaller than that required for turn-off as shown in Figure 1-2c. Under this condition the turn-off voltage will not be sufficient to extinguish the remote filament. Therefore, turn-off cannot occur and the device fails.

3. A Double Gate Layer, Shorted Anode GTO

It is apparent from the analysis of the gate turn-off process that for a reliable gate turn-off the following basic features are desirable:[75-1]

a. A low lateral resistance of the gated base region,

b. A high breakdown voltage for the gate-cathode junction,

c. A non-regenerative section (away from the gate contact) in which the final conducting filament will extinguish itself.

Figure 1-3 depicts a structure in which these essential features are incorporated. A low resistivity p-layer in the gated base provides the low lateral resistance while a higher resistivity p-layer on top, in contact with the cathode junction, assures a high gate-breakdown voltage. In addition, adjacent to the four layer section a non-regenerative section has been included away from the gate contact. The "on-state" condition is shown in Figure 1-3a. It is essentially the same as for the conventional structure. The by-pass current through the three layer NPN transistor section can be negligible with respect

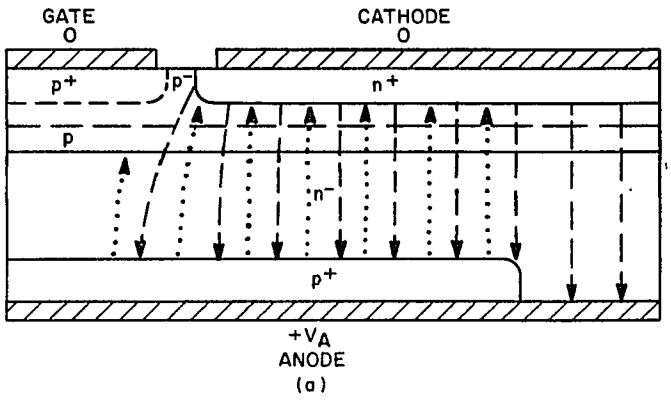

Figure 1-3a. GTO-Thyristor with Buffer Area in "On" State

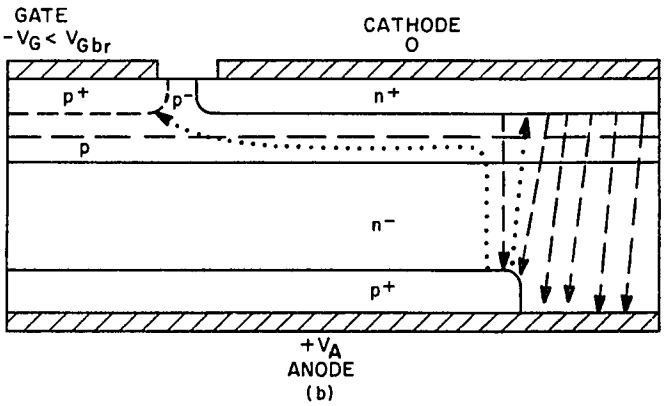

Figure 1-3b. GTO-Thyristor with Buffer Area during Turn-Off

Figure 1-3. Turn-Off Process in GTO Structure with Low Resistance, High Breakdown Gate Layer

to normal rated anode current.[1)]

Upon application of a negative bias to the gate, the plasma is again "squeezed" into a high density filament, as shown in Figure 1-3b. But now, current is deflected into the non-regenerative three layer section and cannot sustain itself. Further, the negative gate (base) current flows through the low resistivity base layer section, producing little lateral voltage drop, while independently the gate-cathode breakdown voltage can be kept high. Thus, avalanching (as depicted in Figure 1-2c) is prevented. As a result, safe turn-off is implemented more readily.

4. Interdigitation, Series Schottky Barrier, and Dynamic Ballasting

A very essential characteristic, desirable for a GTO is to achieve turn-off at a low negative gate voltage.

For turn-off, charge only has to be removed in accordance with the general relation

$$Q_{off} = \int_{t_1}^{t_2} I_A(t)\, dt \qquad 1\text{-}5$$

where Q_{off} is the total charge in the device, t_1 is the time at the onset of the gate turn-off pulse, and t_2 is the instant at which the

[1]This is true only for the case that the width of the cathode is large compared to the size of the shorting N region, see figure 1-3.

sum of the α's is reduced to less than unity at every point within the entire structure, as required by equation 1-3. This process is basically independent of voltage. Thus, the importance of a high gate-cathode breakdown is diminished (feature b discussed in the previous section).

A design which is highly interdigitated or finely subdivided is obviously of advantage. It will minimize lateral sweepout times for minority carriers.

An investigation of the dependence of electrical characteristics on the geometry of a GTO-thyristor (mainly the width of the cathode for constant area) and an explanation of the behavior of such two-dimensional devices is subject of chapter III.

In the course of this work it became apparent that although marked improvements in turn-off were achieved through interdigitation as well as a better understanding of the circuit-device interaction was obtained, the implementation of non-regenerative regions (feature c, sometimes described as "anode shorts" or "by-pass transistors") would greatly impair turn-on performance, especially at low temperatures. A unique concept was introduced by the author by adding a Schottky barrier in series with the bypass transistor to the GTO - structure[79-1] thus negating the adverse effects on turn-on while retaining the improved features for turn-off, independent of cathode width and cathode spacing. Chapter IV-A gives details about these experiments and analyzes the results.

Still, there were burn-out spots due to high current density filaments in the center of the cathode observed. This led to the introduction of the principle of "defocusing" or "dynamic ballasting" [80-1].

Briefly, this method uses a slightly resistive cathode layer, the sheet resistance being closely controlled by ion implantation. The center of the cathode is insulated from the cathode metal. During the "on" state at nominal current densities, the vertical resistance is small and has little effect on the internal forward voltage drop. While the device is being turned off, however, the "squeezing" of current into a narrow, high current density filament is markedly impaired owing to the high lateral emitter resistance and related voltage drops which in turn debias the center of the cathode. Chapter VI-B deals with this aspect of preventing failures in GTO-structures.

II. THEORY OF GATE TURN-OFF IN FOUR LAYER DEVICES

The previous chapter described the condition for turn-off in an NPNP structure in a most general manner; i.e., in terms of the loop gain $G_L \leq 1$ (Equation 1-3) and the turn-off gain G_{gq} (Equation 1-4). However, it was pointed out that these formulae were of little practical value, because the current gains (α_1 and α_2) in an actual device are device geometry and time dependent which we call space-time dependent. Thus, at least, a dynamic two-dimensional model is required to explain physical happenings in the interior of the GTO-thyristor which may relate to the electrical characteristics observed at the terminals.

A. A Two-Dimensional Analytical Model

Duane Wolley[66-1] proposed a two-dimensional, analytical model which contains several important features describing the turn-off for a four layer device.

In Figure 2-1a, the schematic for turn-off is depicted. Initially, the NPNP structure is conducting the current I_A being determined simply by the anode voltage V_A and the load resistance R_L (assuming the "on" resistance of the device $R_i \ll R_L$). A step function is applied to the gate (Figure 2-1b) by closing the switch in the gate lead; i.e., a negative potential at the base of the NPN transistor section will cause a negative gate current I_G to flow and tend to reverse bias the cathode-emitter to a value of $-V_G$. The output response is seen in Figure 2-1c.

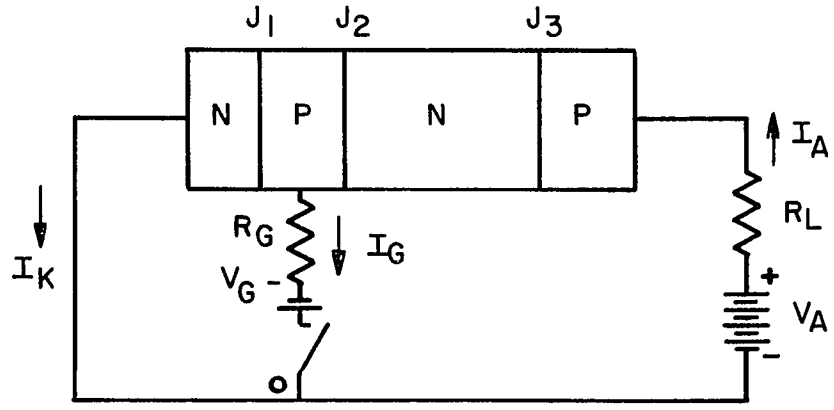

Figure 2-1a. Schematic Circuit Diagram

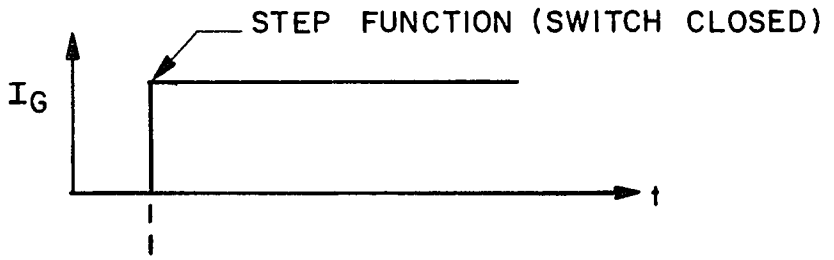

Figure 2-1b. Input Drive Function

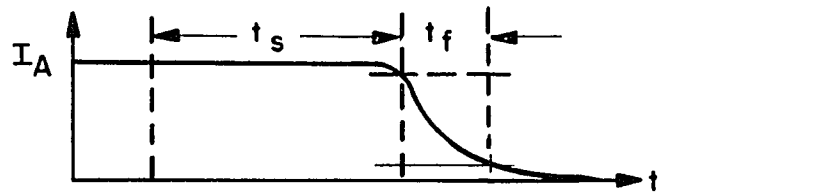

Figure 2-1c. Output Response

Figure 2-1. Conditions for Turn-Off of a GTO

For the duration of the storage time t_s, the anode current remains essentially constant, the minority carrier electron-hole plasma is being "squeezed" toward the center of the device as shown in Figure 2-2. For the duration of the fall time t_f, the plasma density is being reduced by the gate current until the blocking junction J_2 comes out of saturation and the device turns off.

1. The Turn-Off Velocity

In order to obtain a quantitative evaluation for the storage time and fall time, the velocity with which the plasma is squeezed laterally toward the center of the cathode is determined.

The conditions are derived from the model in Figure 2-3. Here, the net rate of removal of minority carriers from an elemental volume ($\Delta x_b w_p L_y$) at the boundary x_b, between the "on" and "off" region is considered; the center is taken as the origin (see Figure 2-3a). The cathode-emitter junction is reverse biased ("off") to the right of Δx_b, i.e., toward the gate with the negative potential applied. It is forward biased ("on") in the region to the left of Δx_b, i.e., toward the center of the emitter.

The gradient of the electron concentration in the "on" region is constant in the z-direction, pure diffusion is assumed for carrier transport across the N-base (see Figure 2-3b).

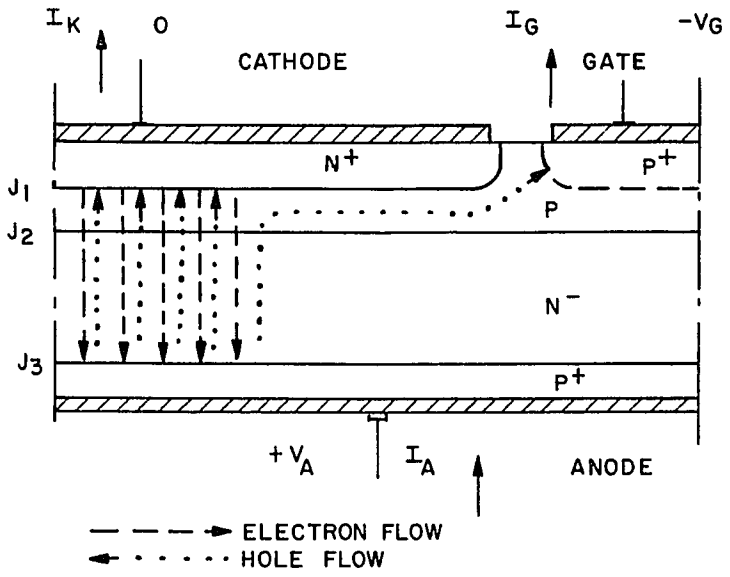

Figure 2-2. Electron-Hole Plasma "Squeezed" Toward Center of Cathode during Turn-Off Process

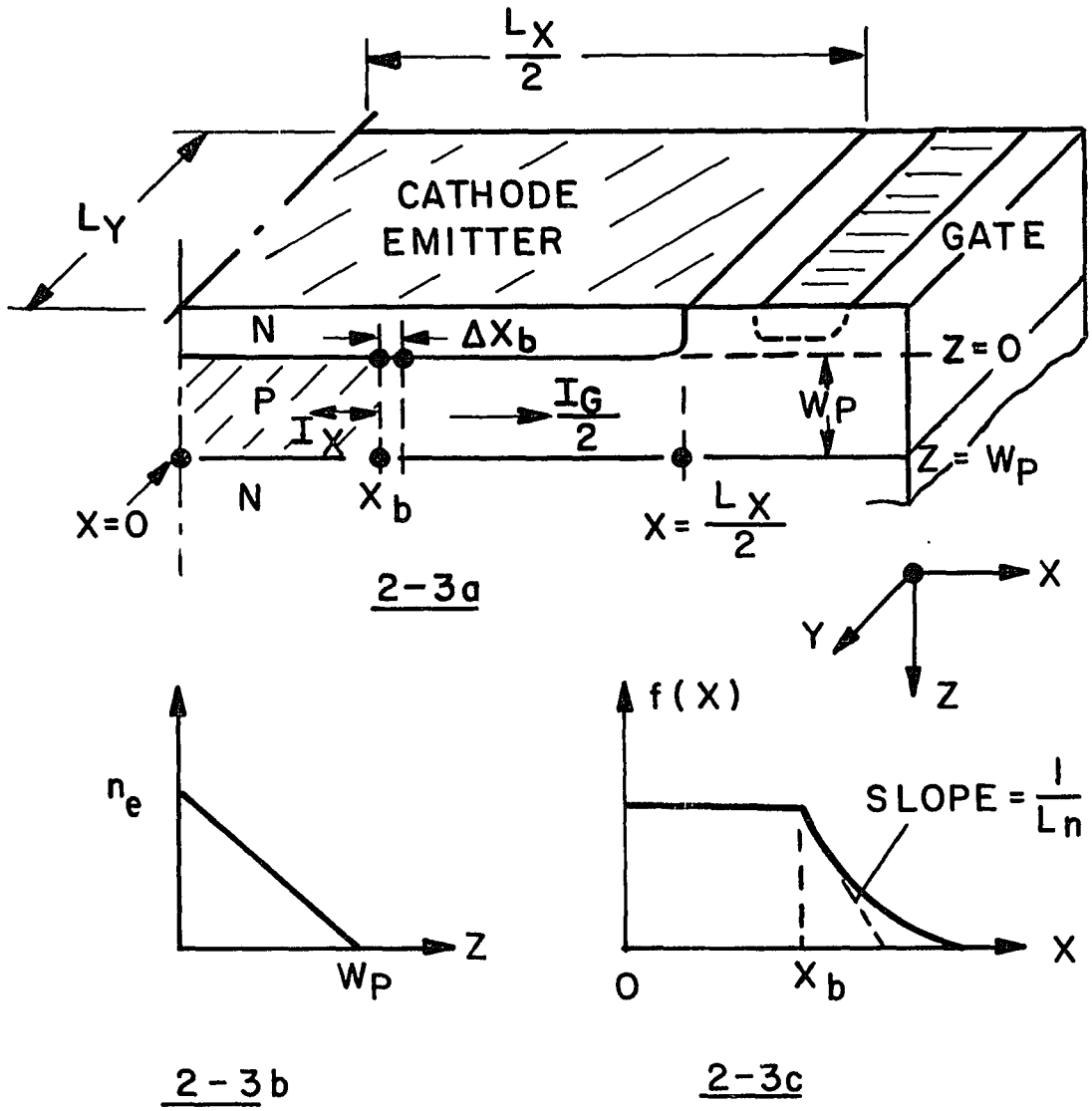

Figure 2-3. Model for Deriving Turn-Off Parameters for a GTO Thyristor (after D. Wolley[66-1])

Figure 2-3a. Two-Dimensional Arrangement

Figure 2-3b. Electron Distribution in Z-Direction

Figure 2-3c. Form Function of Electron Distribution in X-Direction

The removal of minority carriers at the boundary x_b is the gate current $I_G/2$ minus the electron diffusion current into the elemental volume in the x-direction, the magnitude of which is set by the slope $1/L_n$. L_n is defined as an effective diffusion length dependent on electric field, minority carrier lifetime, and ambipolar diffusion coefficient ($L_n = \sqrt{D_n \tau_{eff}}$). Reasonably, L_n is assumed to have the value of the diffusion length for minority carriers in the gated base. Thus, the carrier distribution in the x-direction (lateral) is of the shape f(x) as shown in Figure 2-3c.

The general expression for the minority carrier distribution in the gated base can now be written as

$$n(x,z) = n(x)f(x) \qquad 2\text{-}1$$

Note: The distribution is assumed constant in the y-direction over the length L_y, of the cathode stripe.

The current density in the z-direction is then according to the diffusion part of the minority carrier transport equations

$$J_z(x,z) = qD_n \frac{\partial n(x,z)}{\partial z} \qquad 2\text{-}2$$

and with substituting Equation 2-1 into 2-2

$$J_z(x,z) = qD_n f(x) \frac{\partial n\ (z)}{\partial z} \qquad 2\text{-}3$$

However, since the gradient across w_p is constant (Figure 2-3b)

$$\frac{\partial n(z)}{\partial z} = -\frac{n_e}{w_p} \qquad 2\text{-}4$$

and

$$n(z) = -\int_0^{w_p} \frac{n_e}{w_p}\, \partial z = n_e\,(1-\frac{z}{w_p}) \qquad 2\text{-}5$$

The electron distribution along x as shown in Figures 2-3 is

$$f(x) = \begin{cases} 1 & 0<x\leq x_b \\ e^{-(x-x_b)/L_n} & x_b<x\leq \infty \end{cases} \qquad 2\text{-}6$$

The cathode current is given by

$$I_k = 2I_z = 2L_y \int_0^{\infty} J_z(x,z)dx \qquad 2\text{-}7$$

and using Equations 2-3, 2-4, and 2-6

$$I_k = -2L_y \left[\int_0^{x_b} qD_n \frac{n_e}{w_p}\, dx + \int_{x_b}^{\infty} qD_n \frac{n_e}{w_p} (e^{-(x-x_b)L_n}\, dx \right] \qquad 2\text{-}8$$

The evaluated integral then assumes the form

$$I_k = -2L_y qD_n \frac{n_e}{w_p}\,(x_b + L_n) \qquad 2\text{-}9$$

An important consequence of Equation 2-9 is, that the highest electron concentration will occur in the completely "squeezed" state for $x_b = 0$ at the center of the emitter. The current density is then rising to

$$J_{z(max)} = J_{z(on)}\left(\frac{L_x}{L_n}\ \frac{I_A - I_G}{I_A}\right) \qquad 2\text{-}10$$

where

$$J_{z(on)} = \frac{I_k}{L_x L_y} \qquad 2\text{-}11$$

is the uniform current density throughout the active device area in the "on" state prior to initiation of "turn-off".

For the determination of the lateral diffusion current into the elemental volume $(\Delta x_b w_p L_y)$ we set

$$I_x(x_b) = L_y \int_0^{w_p} J_x(x_b, z)dz \qquad 2\text{-}12$$

where J_x is similarly determined as in Equation 2-2

$$J_x(x_b, z) = qD_n \frac{\partial n\ (x,z)}{\partial x} \qquad 2\text{-}13$$

evaluated at $x = x_b$ yields as seen from Figure 2-3c and condition 2-6

$$J_x(x_b, z) = qD_n\ n(z) f'(x_b) = qD_n\ n(z)\ (-\frac{1}{L_n}) \qquad 2\text{-}14$$

Now, the electron distribution in the z-direction can be substituted from Equation 2-5, which allows Equation 2-12 to be written as

$$I_x(x_b) = -L_y q \frac{D_n}{2L_n} n_e \int_0^{w_p} (1 - \frac{z}{w_p}) d z \qquad 2\text{-}15$$

$$= -L_y q \frac{D_n}{2L_n} n_e w_p$$

The minority carrier charge within the elemental volume is given by

$$\Delta Q = - L_y q \Delta x_b \int_0^{w_p} n(x,z) dz \qquad 2\text{-}16$$

assuming $f(x) \sim f(x_b) = 1$ throughout Δx_b, $n(z)$ may be again substituted from Equation 2-5 resulting in

$$\Delta Q = - L_y q \, n_e \Delta x_b \frac{w_p}{2} \qquad 2\text{-}17$$

Finally, the net change of charge in the elemental volume with time is the sum of the (conventional) diffusion current $I_x(x_b)$ and the gate current $I_G/2$, i.e.,

$$\frac{\Delta Q}{\Delta t} = I_x + \frac{I_G}{2} \qquad 2\text{-}18$$

Substituting Equations 2-15 and 2-17 into Equation 2-18 gives

$$-L_y q n_e \frac{\Delta x_b}{\Delta t} \left(\frac{w_p}{2}\right) = -L_y q \frac{D_n}{2L_n} n_e w_p + \frac{I_G}{2}$$

then solved for $\Delta x_b/\Delta t$ is

$$\frac{\Delta x_b}{\Delta t} = \frac{D_n}{L_n} - \frac{I_G}{L_y q n_e w_p} \qquad 2\text{-}19$$

An explicit expression for the turn-off velocity is obtained by solving Equation 2-9 for the electron concentration at the cathode emitter edge (z=0) and substituting it into Equation 2-19; with $\Delta x_b \to 0$ we obtain

$$\frac{dx_b}{dt} = \frac{D_n}{L_n} + \frac{I_G}{I_k}\left(\frac{2D_n}{w_p^2}\right)(x_b + L_n) \qquad 2\text{-}20$$

The cathode current during turn-off is

$$I_k = I_A - I_G \qquad 2\text{-}21$$

and the transit time for carriers through the base can be expressed as

$$t_p = \frac{w_p^2}{2D_n} \qquad 2\text{-}22$$

further, with the turn-off gain as defined in Equation 1-4

$$G_{gq} = \frac{I_A}{I_G} \qquad 2\text{-}23$$

we can write Equation 2-20 as follows

$$\frac{dx_b}{dt} = \frac{x_b + L_n}{t_p\,(G_{gq}-1)} + \frac{D_n}{L_n} \qquad 2\text{-}24$$

2. The Storage Time and Maximum Turn-Off Gain

The storage time t_s is essentially the time it takes to squeeze the electron-hole plasma from its original uniform flow through the entire device cell of length L_y and width L_x into a filamentary line of width $2L_n$. One can therefore integrate equation 2-24 in x between the limits $L_x/2$ and L_n,

$$-\int_0^{t_s} dt = t_p\,(G_{gq}-1) \int_{L_x/2}^{L_n} \frac{dx_b}{x_b+L_n-t_p(G_{gq}-1)D_nL_n} \qquad 2\text{-}25$$

which results in

$$t_s = t_p(G_{gq}-1)\ \ln \frac{\left(2L_xL_n/w_p^{\,2}\right) + \left(2L_n^{\,2}/w_p^{\,2}\right) - G_{gq}+1}{\left(4L_n^{\,2}/w_p^{\,2}\right) - G_{gq}+1} \qquad 2\text{-}26$$

The storage time t_s approaches infinity when the denominator of the logarithmic term in Equation 2-26 goes to zero, i.e., we obtain for the maximum turn-off gain

$$G_{gq(max)} = \frac{4L_n^{\,2}}{w_p^{\,2}} + 1 \qquad 2\text{-}27$$

Equation 2-26 can be used to calculate the storage time as a function of turn-off gain. The results of such calculations are depicted in Figure 2-4 using the lateral diffusion length L_n as parameter. As can be seen, the storage time is a strong function of the turn-off gain. It should be noted that this turn-off gain is set by the external input circuit and output circuit conditions (see Figure 2-1a) and is limited by the internal device impedance. The turn-off gain of the one-dimensional device (i.e., in the "squeezed" state) is still governed by Equation 1-4. Thus, it is apparent that the smaller of the two values, which is obtained from either Equation 1-4 or Equation 2-27, becomes the limiting gain.

3. The Lateral Base Resistance and Maximum Turn-Off Anode Current

The lateral gate current I_G during turn-off causes a voltage drop along the cathode emitter junction. This voltage drop may reach the cathode-gate breakdown voltage as observed by van Ligten and Navon[60-1] and limit the allowable current to be turned off. For the device model of Figure 2-3a the maximum lateral gate resistance is experienced when the "on" region is reduced to its minimum width of $2L_n$. Thus, this lateral gate resistance beneath the half width $L_x/2$ of the cathode emitter is determined as

$$R_g = \bar{\rho}_P \frac{\frac{L_x}{2} - L_n}{w_p L_y} \qquad 2\text{-}28$$

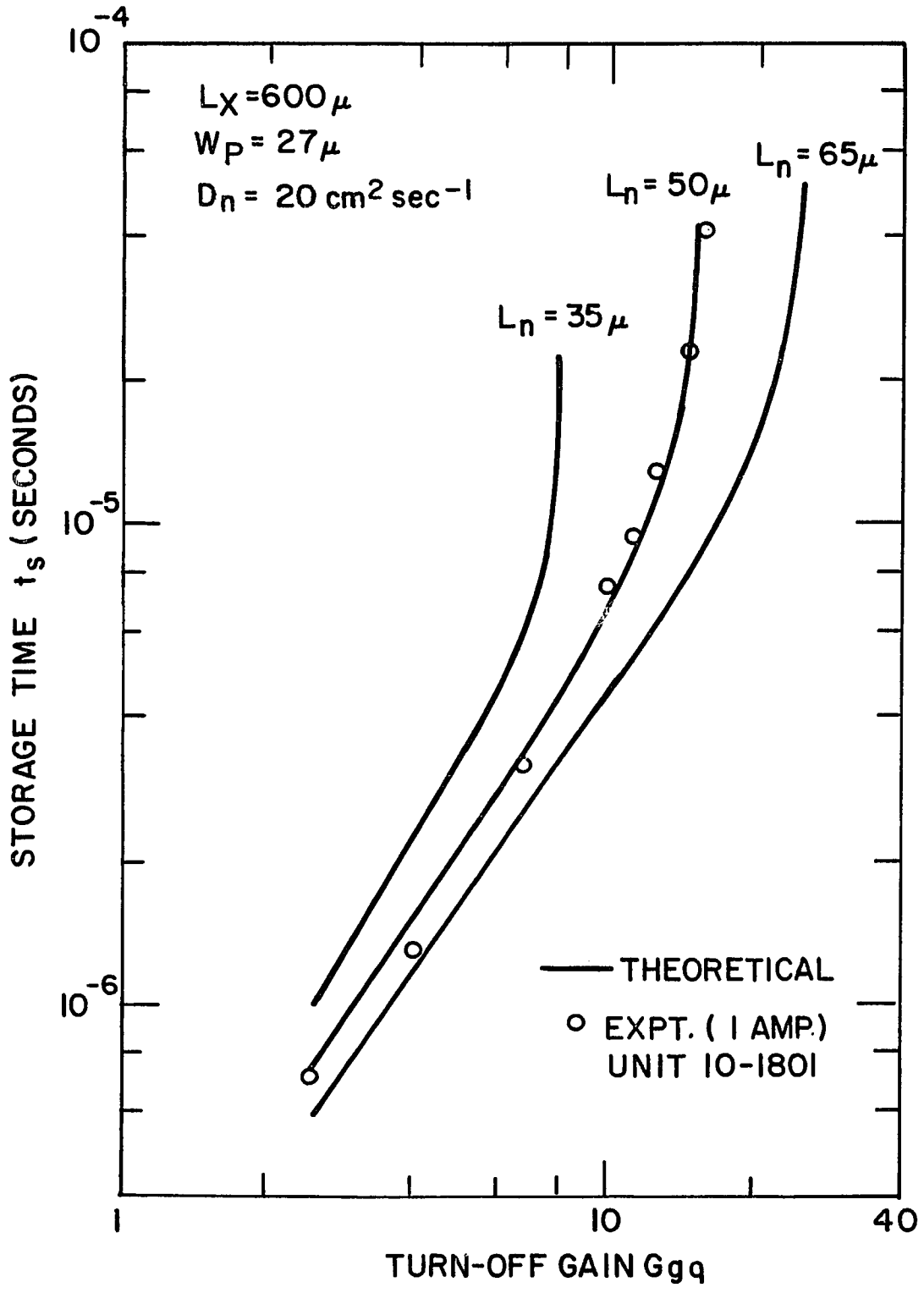

Figure 2-4. Storage Time vs. Turn-Off Gain (after D. Wolley[66-1])

where $\bar{\rho}_p$ is the average resistivity of the unmodulated, active gate region. Because of the restriction (see Figure 1-2c)

$$\frac{I_G}{2} R_g < V_{G\ br} \qquad 2\text{-}29$$

where $V_{G\ br}$ is the gate-cathode breakdown voltage, there exists an upper limit for the anode current that can be turned off. With the assumption that $(L_x/2) >> L_n$ it then follows from Equations 2-23, 2-28, and 2-29, that

$$I_{A(max)} = \frac{4\ G_{gq}\ V_{Gbr} w_p L_y}{\bar{\rho}_p L_x} \qquad 2\text{-}30$$

4. The Fall Time

The fall time is determined by the time required to remove the charge from the volume of the device after the center junction comes out of saturation and becomes reverse biased. The negative gate current aids the removal of carriers, the time constant is short as for transistors with negative base drive. However, the charge in the ungated base (N^-) section must either drift or diffuse to the center junction and be collected there, or recombine with majority carriers. It then follows that there is generally a second time constant associated with the turn-off of a GTO thyristor. This second time constant causes a so-called "tail" in the turn-off characteristic and it is a function of the lifetime of minority carriers in the ungated base[75-1]. An example for the output current-input current response with time is given in Figure 2-5.

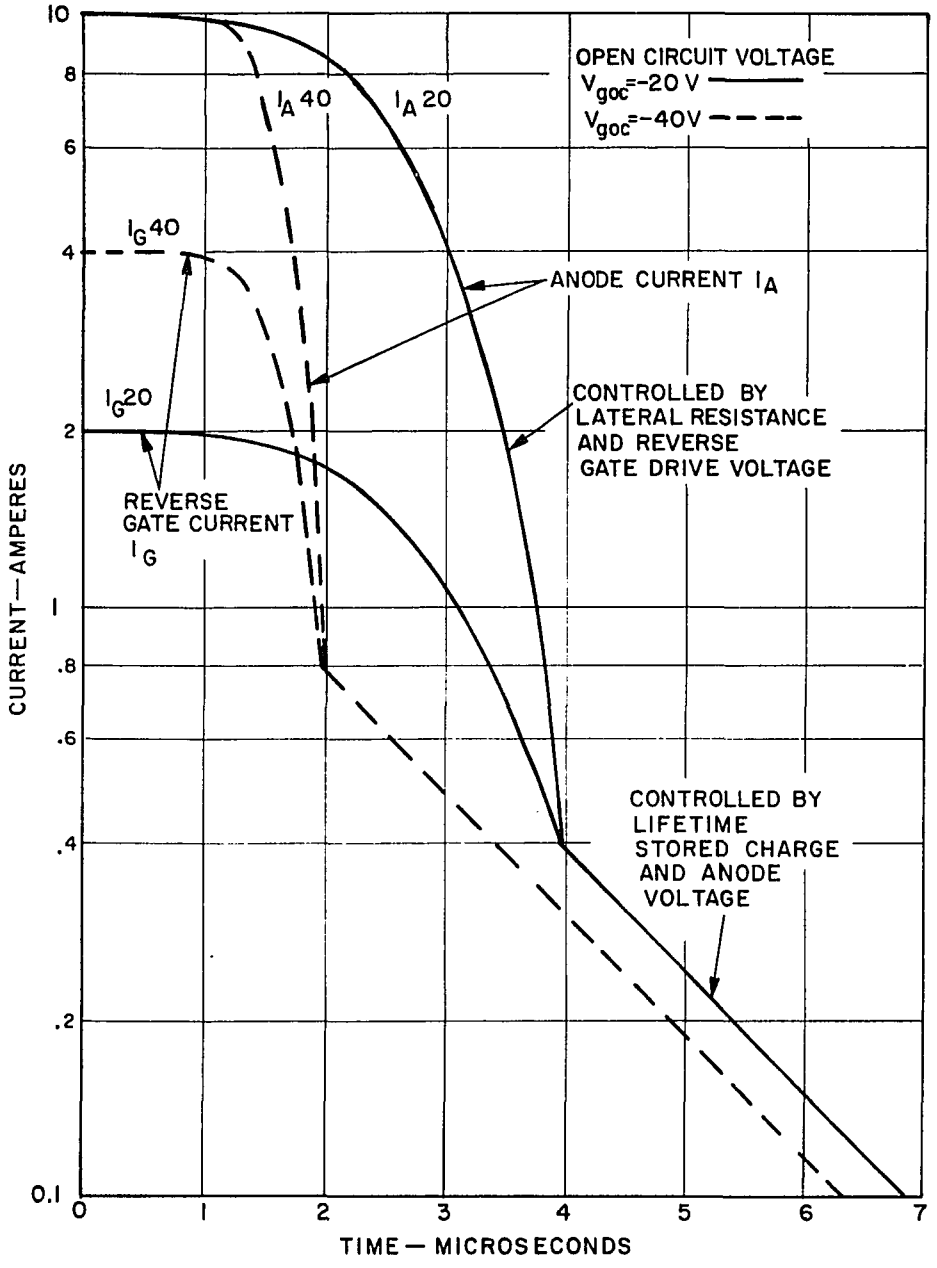

Figure 2-5. Input Current I_G and Output Current Response I_A as Function of Time for GTO-Thyristor During Turn-Off[75-1]

B. A Two-Section, Charge Control Model

1. The Charge Control Concept

Mamuro Kurata[74-1] developed a CAD-model for turn-off using the charge control approach. This procedure was originally described by Beaufoy and Sparks[57-1] for transistors, and later applied by Davies and Petrucella[67-2] to thyristors. Here, the basic idea is to take the current continuity equation, for example, as given below in one dimension for an NPN transistor

$$\frac{\partial I}{\partial z} = q \frac{\partial n(z)}{\partial t} + q \frac{n(z)}{\tau_B} \qquad 2\text{-}31$$

and integrate it across the base, i.e., between the limits $z = 0$ and $z = W_p$, after multiplying both sides by ∂z. The result is

$$I_B = \frac{d\, Q_N}{dt} + \frac{Q_N}{\tau_B} . \qquad 2\text{-}32$$

Thus, in equation 2-32 for the base current I_B the carrier density $n(z)$ as a variable is now replaced by the total excess charge Q_N in the base, its spatial distribution does not enter.

Equation 2-32 may be adapted to a thyristor element N, such that the charge control conditions describe the carrier dynamics in the vertical (z) direction. Adjacent elements, laterally interconnected by appropriately modeled base resistances to include conductivity modulation, can then be used to set up a two-dimensional, numerical simulation for turn-off.

However, let us first consider the four layer structure of Figure 1-1a and 1-1b and label the currents as shown in Figure 2-6. The resultant expressions for the NPN transistor section and PNP transistor section are in accordance with Equation 2-32

$$I_1(N+1) - I_1(N) + I_{C2}(N) = \frac{d\,Q_1(N)}{dt} + \frac{Q_1(N)}{\tau_{B1}} \qquad 2\text{-}33$$

and

$$I_2(N) - I_2(N+1) + I_{C1}(N) = \frac{d\,Q_2(N)}{dt} + \frac{Q_2(N)}{\tau_{B2}}\,, \qquad 2\text{-}34$$

respectively.

For the numerical treatment of the turn-off process, Equations 2-33 and 2-34 assume different forms as the thyristor element N transits from the saturation condition, in the "on-state", through the non-saturation phase, where both transistors are in the active region, into the depletion state. For mathematical details and assumptions we refer to M. Kurata's original treatment[74-1].

2. The Junction Voltages

Next, "some relations must be assumed between the base charges Q(N) and the junction voltages $V_j(N)$, to obtain a self-consistent device model". For the cathode junction J_1 during the conducting state a low, constant voltage is assumed. During reverse blocking, however, a depletion layer is formed. This depletion layer can be interpreted as a negative charge, the voltage developed across being proportional to the total number of fixed charges, the junction capacitance is assumed constant.

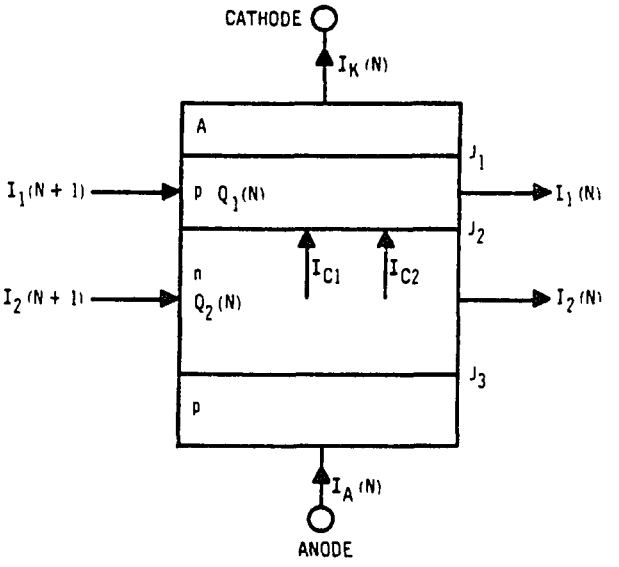

Figure 2-6a. Thyristor Element N

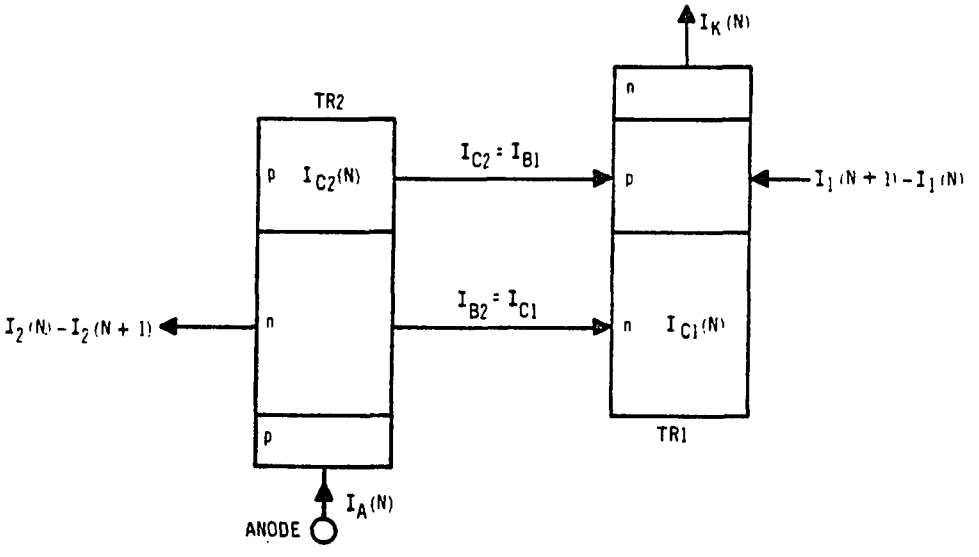

Figure 2-6b. Two Transistor Equivalent

Figure 2-6.
Thyristor Model for Definition of Charge Control Equation

Therefore, plotting $V_{j1} = f(Q_1)$ results in two asymtotes. $V_{j1} = V_{j10}$ = constant for positive Q_1, and $V_{j1} = (Q_1/C_{j1}) + V_{j10}$ for negative Q_1 as depicted in Figure 2-7. The actual dependence of V_j on Q is then obtained from a curve fitting method such that the requirement $V_j \to 0$ for $Q \to 0$ is met. The result can be expressed as

$$V_{j1}(N) = \frac{Q_1(N)}{2C_{j1}(N)} + V_{j10}(N) - \sqrt{\left(\frac{Q_1(N)}{2C_{j1}(N)}\right)^2 + V_{j10}^2(N)} \qquad 2\text{-}35$$

which is also plotted in Figure 2-7.

The relation for the anode junction $V_{j3}(N)$ is of the same form.

$$V_{j3}(N) = \frac{Q_2(N)}{2C_{j3}(N)} + V_{j30}(N) - \sqrt{\left(\frac{Q_2(N)}{2C_{j3}(N)}\right)^2 + V_{j30}^2(N)} \qquad 2\text{-}36$$

The voltage across the center junction can be expressed as

$$V_{j2}(N) = \sqrt{\left(\frac{f(N)}{2C_{j2}(N)}\right)^2 + V_{j20}^2(N)} - \frac{f(N)}{2C_{j2}(N)} \qquad 2\text{-}37$$

where f(N) has the dimension of a charge consisting of two parts, an injection component during conduction, represented by the product of a current and a transit time, and a depletion charge, given by the product of a capacitance and voltage. Again, for details we refer to Ref. 74-1.

3. The Current Loop Equations

Finally, the loop equations are set up. The device structure shown in Figure 2-8 is subdivided into two sections and can be represented by an equivalent schematic as is shown in Figure 2-9.

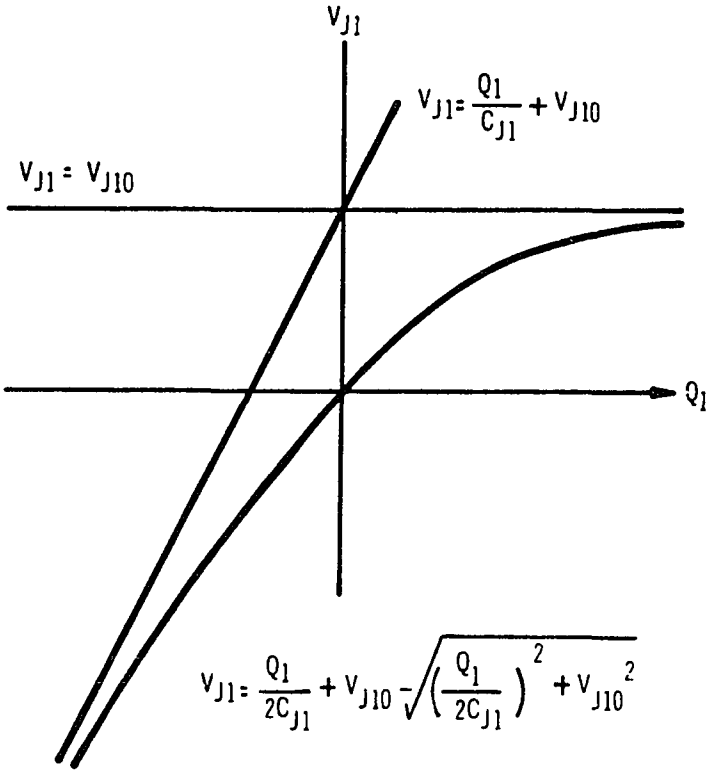

Figure 2-7.
Voltage vs. Charge for Cathode Junction J_1, or Anode Junction J_3 (after M. Kurata)[74-1]

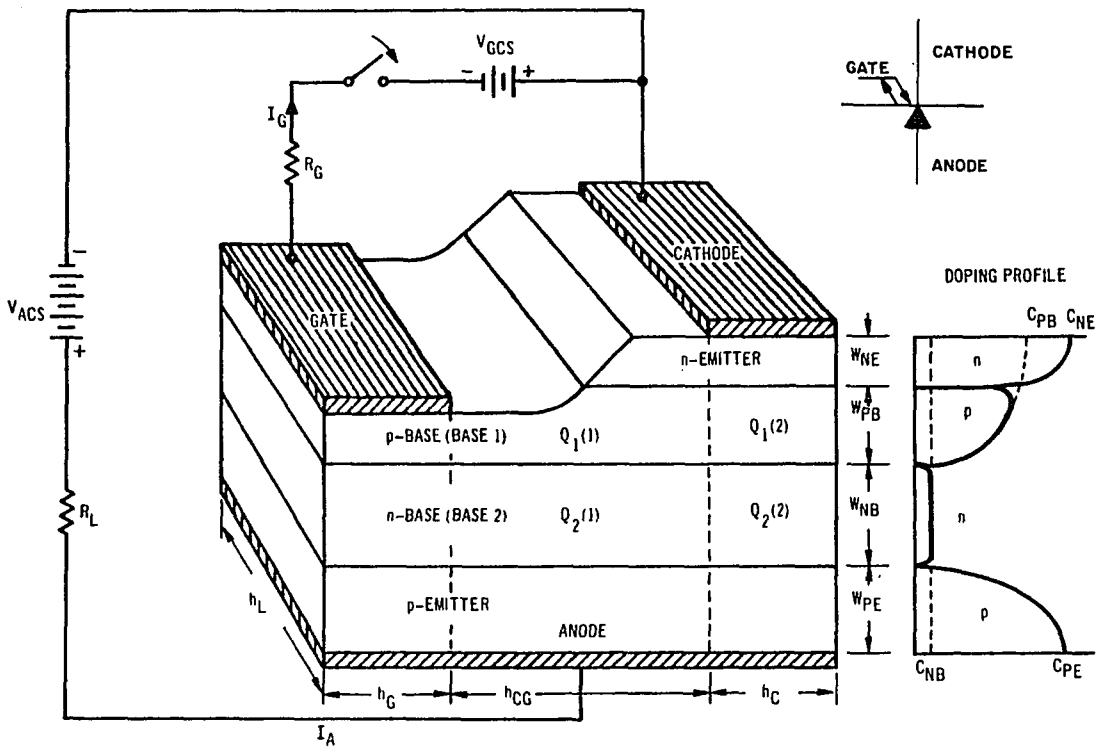

Figure 2-8.
GTO Two-Section Model
(after M. Kurata)[74-1]

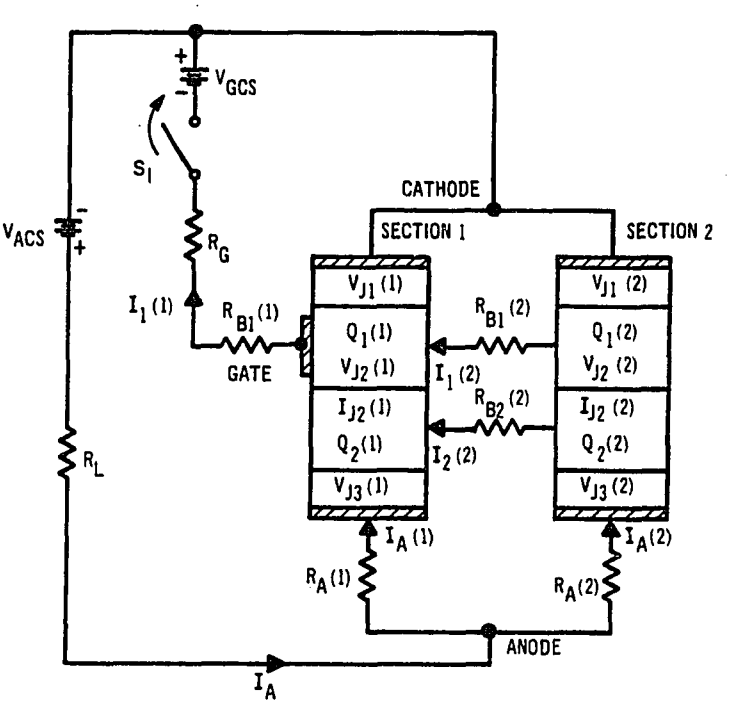

Figure 2-9.
Equivalent GTO-Thyristor Circuit for Two-Section Model (after M. Kurata)[74-1]
Closing S_1 initiates Turn-off

The loop equations are thus

$$V_{j1}(1) = -V_{GCS} + [R_{B1}(1) + R_G]\, I_1(1) \qquad 2\text{-}38$$

$$V_{j1}(2) = V_{j1}(2) + R_{B1}(2)I_1(2) \qquad 2\text{-}39$$

$$V_{j2}(2) + R_{B1}(2)I_1(2) = V_{j2}(1) + R_{B2}(2)I_2(2) \qquad 2\text{-}40$$

$$V_{j1}(1) + V_{j2}(1) + V_{j3}(1) + R_A(1)I_A(1) + R_L[I_A(1) + I_A(2)]$$

$$= V_{ACS} \qquad 2\text{-}41$$

$$V_{j1}(2) + V_j2(2) - V_j3(2) + R_A(2)I_A(2) + R_L[I_A(1) + I_A(2)]$$

$$= V_{ACS} \qquad 2\text{-}42$$

Equations 2-33 to 2-42 are the basis for a thyristor model, the turn-off behavior of which may be calculated by a numerical approach.

4. The Computation Method

For the numerical solution we first choose the appropriate form of the charge control equations 2-33 and 2-34, dependent whether the device section considered is in saturation, the active transistor mode, or in reverse bias, i.e., in the depletion state. Then, the expressions for the junction voltages in equations 2-35, 2-36 and 2-37 are substituted into equations 2-38 and 2-41 for N = 1, and in equations 2-39, 2-40, and 2-41 for N = 2, respectively.

Therefore, a total of 9 equations with 9 variables has to be solved simultaneously for this two-section model[1].

Because the charges as well as the currents are non-linear, an iterative scheme (Newton-Raphson's principle) is utilized, i.e., the variables $Q_1 \sim I_2$ are replaced by $(Q_1 + \delta Q_1) \sim (I_2 - \delta I_2)$ etc. The result is a system of linear equations containing the variables $\delta Q_1(1)$, $\delta Q_1(2)$, $\delta Q_2(1)$, $\delta Q_2(2)$, $\delta I_A(1)$, $\delta I_A(2)$, $\delta I_1(1)$, $\delta I_1(2)$, and $\delta I_2(2)$, the solution of which can be obtained by application of the Gaussian elimination method. This set of solutions is valid for one instant of time, and is repeated at suitably spaced intervals until $I_A \to 0$. The steady state solution, i.e., $dQ_1(N)/dt = 0$ and $dQ_2(N)/dt = 0$ in equations 2-33 and 2-34, provides the initial conditions for the transient solutions.

5. Base Charges and Currents During Turn-Off

We will now look at an example for turn-off. The intention is not to discuss the validity of the quantitative values obtained, but rather to observe the relative distribution of charges and currents as a function of time in both device sections.

Necessary input parameters are the doping profile, lateral dimensions of the device structure, lifetimes in the base regions τ_{B1} and τ_{B2}, anode and source voltages V_{ACS} and V_{GCS}, and the external resis-

[1] For a model containing M sections, a total of (5M-1) simultaneous equations must be solved.

tances R_L and R_G.

For a typical triple diffused thyristor profile as shown on the right hand side of Figure 2-8 the surface concentrations and vertical dimensions are: $C_{NE} = 4 \times 10^{21}$, $C_{PB} = 3 \times 10^{18}$, $C_{NB} = 2 \times 10^{14}$, $C_{PE} = 3 \times 10^{18}(cm^{-3})$, and $W_{NE} = 10$, $W_{PB} = 40$, $W_{NB} = 150$, $W_{PE} = 30(\mu)$, respectively.

The lifetime in the P-base is assumed $\tau_{B1} = 5\mu s$, whereas in the N-base $\tau_{B2} = 2.5\mu s$.

For lateral dimensions the following values are chosen (see Figure 2-8): $h_C = 200$, $h_G = 200$, $h_{CG} = 100(\mu)$ and the length of the device is $h_L = 4000\mu$. Further, $V_{ACG} = 200V$, $V_{GCS} = 10V$, $R_L = 250\Omega$, and $R_G = 100\Omega$.

Assuming for the collector time constants the low injection value

$$\tau_C = 2\tau_B \left[\sinh^2\left(\frac{W_B}{2L_B}\right)\right], \qquad 2\text{-}43$$

the one dimensional turn-off gain can be determined from

$$G_{gq} = \frac{1 + \tau_{C2}/\tau_{B2}}{1 - (\tau_{C1}/\tau_{B1})(\tau_{C2}/\tau_{B2})} \qquad 2\text{-}44$$

which can be shown to be identical to Equation 1-4.

Using the given input data and a turn-off gain of 10 we obtain the results plotted in Figure 2-10. Figure 2-10a shows the base charges. We notice, the excess charge in the P-base $Q_1(1)$ of section 1 is extracted fast, i.e., the N-emitter is shut off in this region. The

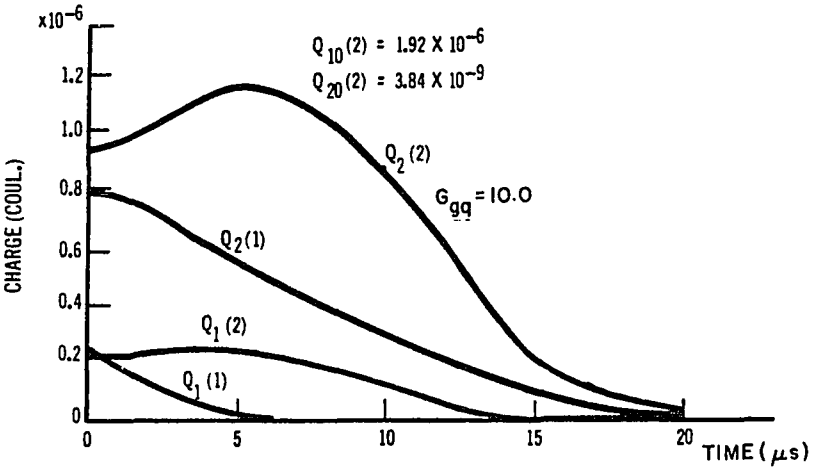

Figure 2-10b. Current Components vs. Time

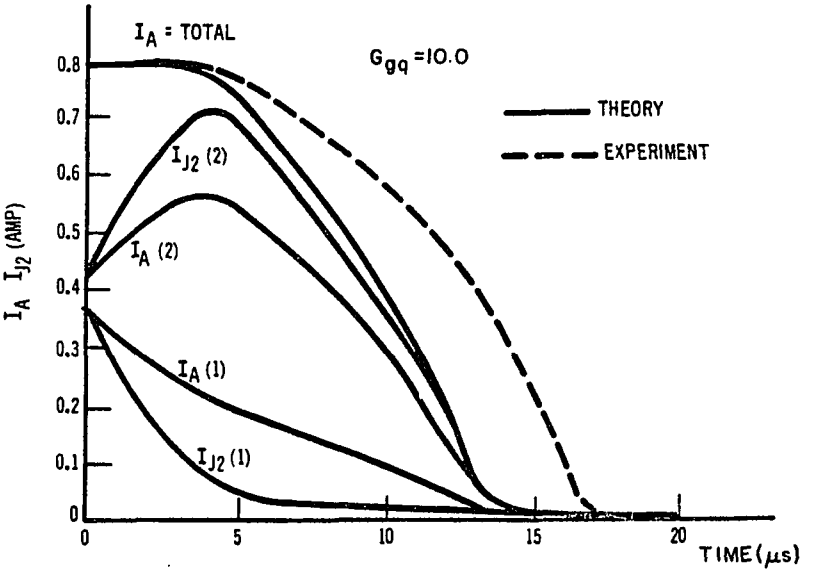

Figure 2-10a. P-Base Charge and N-Base Charge vs. Time

Figure 2-10.
Base Charges and Anode Current for Two-Section GTO-Thyristor Model during Turn-off (After M. Kurata)[74-1]

charge in the N base $Q_2(1)$ is swept out into Section 2. Indeed $Q_2(2)$ increases initially and $I_{j2}(2)$, the current through the center junction of this section, is larger than the anode current $I_A(2)$ throughout the turn-off phase as seen in Figure 2-10b. Most of the anode current $I_A(1)$ injected into section 1 flows laterally to the center of section 2.

The important feature to notice is that, while the total anode current I_A remains constant, the current in section 2 increases appreciably, and peaks about the time $Q_1(1)$ vanishes. This phenomena very clearly demonstrates the "squeezing" of the conduction area into a filament, similarly as assumed for D. Wolley's analytical model[66-1]. In Kurata's approach, the charge in the N-base and conductivity modulation is included, however. Further, the time-dependent current wave form $I_A(t)$ by and large resembles that seen for actual devices, although a pronounced recombination tail (see Figure 2-5) is not produced[1].

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[1] Of interest here is a one-dimensional analysis of turn-off phenomena by M. Naito et al [79-3]. In this analysis an exact numerical solution of a full set of semiconductor equations including high injection effects is used and turn-off waveforms can be remarkably well simulated. Though this one-dimensional model does provide "a great deal of insight into the device's operation", it does not lend itself to aid in solving problems concerning current filamentation, and device failures due to excessively high local current densities during turn-off.

[2] D'yakonov and Levinshtein[80-2] have made calculations "of the maximum value of the density of minority carriers in a filament and of their spatial distribution as a function of the turn-off gate current". Their theory ignores injection during the turn-off process, i.e., in Equation 1-5, the total charge Q_{off} would be $Q(t_1)$, no further charge is added. A reference to time is absent. Thus, standing filaments, heating and burn-out failure cannot be predicted. Yet, the treatment in 80-2 points toward filament formation in support of Wolley's and Kurata's theories.

III. A HIGH SPEED, HIGH VOLTAGE EPI-BASE STRUCTURE[1]

Progress in semiconductor technology and process control have made it possible to obtain reasonably tight tolerances for the physical parameters of multilayer semiconductor structures. Also, the possibility to use the digital computer for the artwork generation of photomasks have made it feasible to produce multiple patterns of different devices, side by side, on the same wafer. These facts were applied to investigate the dependence of the electrical characteristics for vertically identical GTO structures as a function of the horizontal geometry. They are described in this chapter in some detail.

A. Motivation

In the introduction it was mentioned that it would be desirable to combine the features of a transistor and a thyristor for obtaining an electronic switch offering advantages over either types of these conventional devices. The incentive to investigate such a transistor-thyristor hybrid becomes apparent by considering the internal loss, i.e., the power dissipation of a device chip as a function of the average current density.

Figure 3-1 illustrates the general trend. In this figure we observe two bands of rising power dissipation, one for transistors the other for thyristors, intersecting each other.

In particular, transistors have small losses at low current densities. The dissipation rises rapidly for average collector current densities exceeding $30A/cm^2$.

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[1] A summary of preliminary results is presented in Reference 77-2.

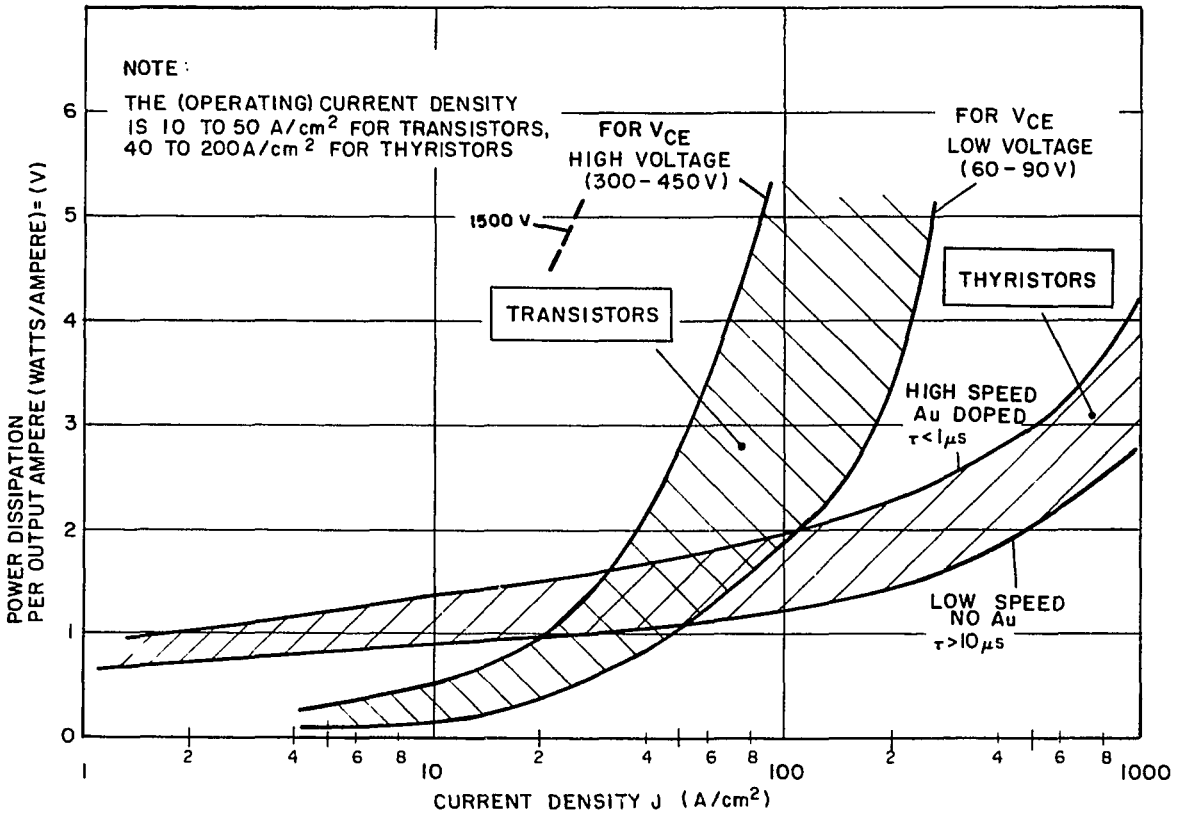

Figure 3-1. Comparison of Power Transistors and Thyristors as an Electronic Switch showing Power Loss in "On" State

J is Average Collector Current Density and Anode Current Density for Transistors and Thyristors, respectively

It is obvious that for high voltage transistors the dissipation is more severe (left hand border of the region) than for low voltage types (right hand border). High voltage transistors have a relatively thick, high resistivity region. Base widening occurs and a pronounced quasi-saturation characteristic causes a marked increase of the collector saturation voltage and a rapid current gain fall-off. It should be noted that considerable base (drive) dissipation is added to the collector loss at high current densities, above $50A/cm^2$.

In contrast, thyristors have some initial dissipation at low current densities because of the additional voltage drop due to the anode junction (0.7 to 0.9 volts for silicon). However, the internal voltage drop remains low as the current density is increased. The power dissipation for thyristors crosses the transistor regions in the neighborhood of 20 to $100A/cm^2$ and then remains below that for higher current densities. The reason for this lower dissipation is of course the conductivity modulation of the high resistivity active regions due to electron-hole injection, and the absence of any gate dissipation in the conducting state due to the regenerative property. Further, it should be pointed out that because of the conductivity modulation, the power dissipation for thyristors is relatively independent of the (blocking) voltage capability.

The losses are effected by the minority carrier lifetime, however. For the on-state, the smaller the lifetime the greater the losses.

For high lifetimes, where diffusion is the major carrier transport mechanism, the lower limit of the dissipation region is approached. This fact applies to low frequency devices as indicated in Figure 3-1.

For high frequency devices the lifetime has to be decreased in order to minimize switching losses, for instance, through deliberate introduction of minority carrier traps by means of gold diffusion[66-2, 72-1]. Then, carrier transport is partially aided by a drift field, at the expense of an additional voltage drop. Thus, a higher dissipation results during the on-period, and the upper boundary of the thyristor region in Figure 3-1 is approached.

We may conclude from the foregoing discussion and Figure 3-1 that for operating a switch above average chip current densities of $50A/cm^2$ with low on-state dissipation a thyristor-like structure is mandatory.

Figure 3-2 attempts to compare the power switching capability with respect to device cost $(VA/\$)$[1] as a function of the frequency for a switch mode power supply using either thyristors or transistors.

We observe that it is possible to switch about 30,000 volt amperes per dollar with thyristors. However, applications are in general limited to low frequencies. Expensive, bulky components, including

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[1] It should be noted that the boundaries designating the VA/$ regions for thyristors and transistors were arrived at by taking the performance data and the sales price (100-999 quantities) for a large number of commercial and industrial devices from various manufacturers several years ago, and assuming arbitrarily a 40% margin. Though the price structure may have changed since that time, the relative relation is still valid.

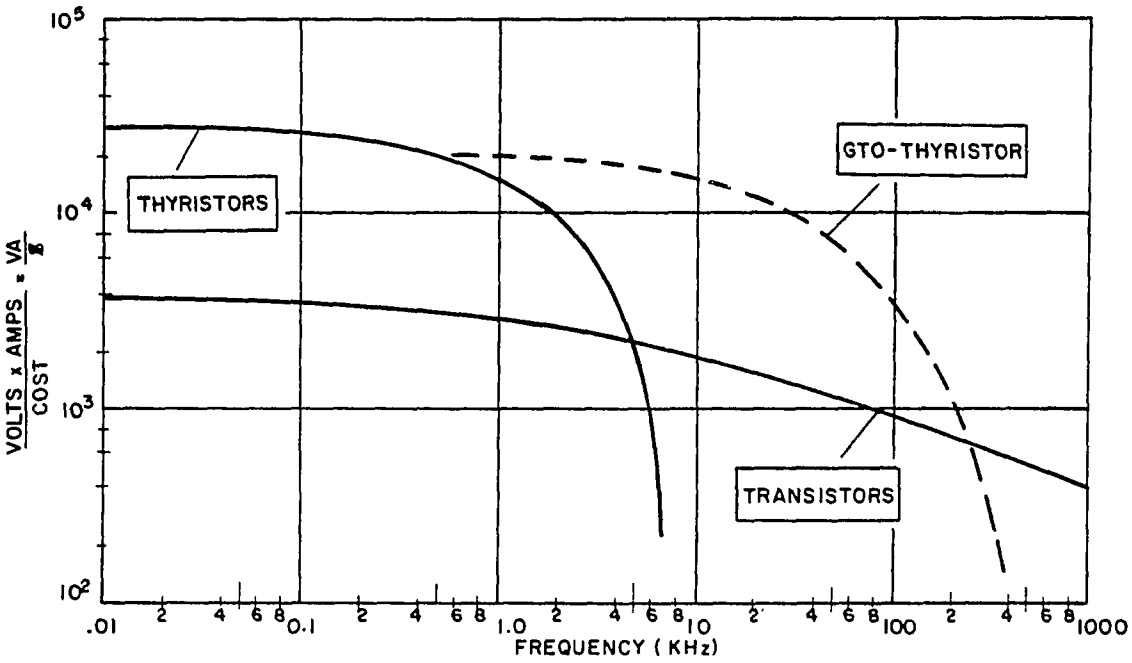

Figure 3-2. Comparison of Power-Switching Capability with Respect to Cost as a Function of Frequency for Thyristors, GTO's, and Transistors

additional active devices for commutation are required. This results in excessive weight and high cost for the total system.

On the other hand, transistors will allow switching at higher frequencies. Yet, the device geometries are more complicated, voltages are limited, dissipation becomes a problem, as shown in Figure 3-1 before. A switching capability of about 1200 volt amperes per dollar is feasible at a frequency of 50kHz according to the transistor performance curve in Figure 3-2. There are fewer circuit elements necessary, and they are lighter and less expensive. The total system is simpler and cheaper, but the attainable volt ampere product per dollar is small. Therefore, very high power conditioning equipment usually employs thyristors operating at low frequencies, while small power supplies can be made with simple transistor circuits.

Again, a gate turn-off device suggests itself as an economical solution to improved performance. A higher power switching capability should be obtained approaching that of thyristors at frequencies similar to those realized with transistors as indicated by the dashed curve in Figure 3-2. A GTO can be controlled for turn-off as well as for turn-on from the gate electrode without commutating the output current and removal of the output voltage, making possible comparable circuit simplicity as for transistors.

B. Choice of Vertical Structure

For the design of the vertical structure of a GTO choices and compromises as are valid for transistors and thyristors have to be applied. The impurity profile comprises the superposition of the donor and

acceptor concentration achieved by means of multiple diffusion steps, epitaxial crystal growth, and the initial, high resistivity starting material.

1. Gate Sheet Resistance

Of paramount importance for a GTO is a low lateral resistance of the active, gated base region (see Figure 1-2c, pp. 8, and Equation 2-30, pp. 27) while maintaining a reasonably high gate-cathode breakdown voltage. The various options are depicted in Figure 3-3.

Figure 2-3a shows the conventional double diffused profile of the gated NPN section in terms of absolute donors and acceptors shown at left, and the resulting net impurity profile shown to the right. The gate conductivity as well as the gate breakdown voltage are very sensitive to variations of x_{j1}. Because of the graded base having a rapid concentration fall-off and high value at the intersection where $|N_A|=|N_D|$, one obtains usually a high base sheet resistance R_{sp} and a low breakdown voltage V_{Gbr}.

Figure 3-3b shows an epitaxially grown gate layer and a diffused cathode, resulting in a "quasi" uniform base. Here, the dependence of gate sheet resistance and breakdown voltage on variations of x_{j1} is less pronounced. Also, assuming the same base width $(x_{j2}-x_{j1})$ as for the illustration of Figure 3-3a, the square profile and a lower concentration crossover allow for a decrease in gate resistance and an increase in breakdown voltage.

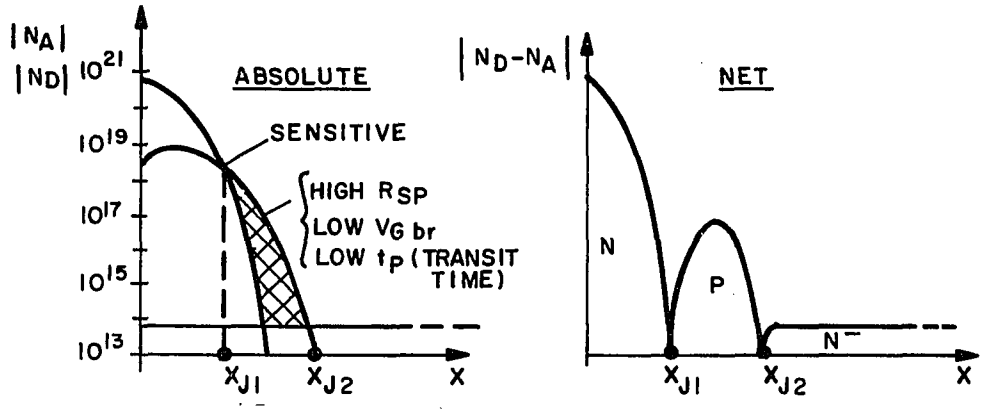

Figure 3-3a. Graded Base (double diffused)

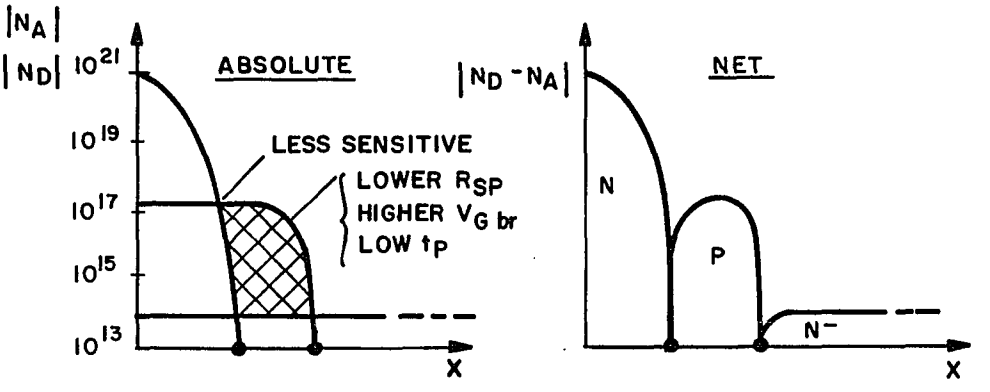

Figure 3-3b. Uniform Base (epitaxial)

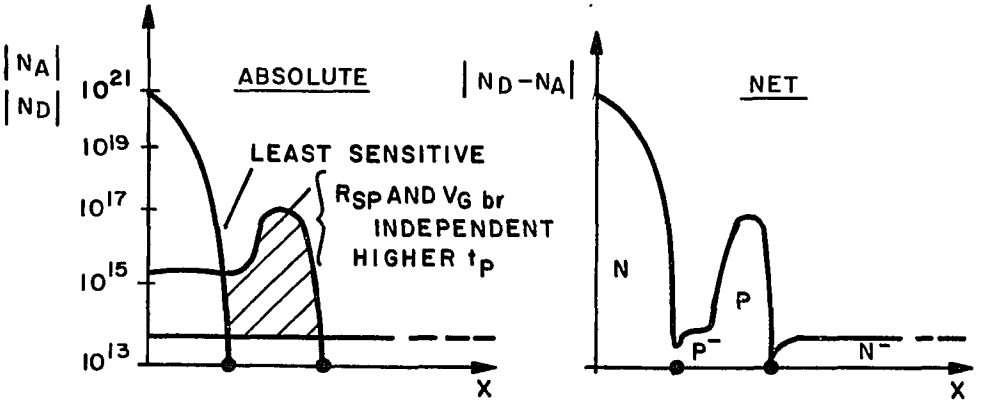

Figure 3-3c. Inverted Base (epitaxial; ion implanted and diffused)

Figure 3-3. Impurity Concentration Profiles for GTO-SCR Structures

Finally, Figure 3-3c shows the case where initially a precise amount of gate impurities is implanted into the substrate. Then, a diffusion followed by an epitaxial deposition of a high resistivity portion forms a double gate layer (see also Figure 1-3, pp. 10). We may easily recognize that here the gate sheet resistance and breakdown voltage are very insensitive to variations of x_{j1}, provided the crossover remains in the high resistivity portion. For this inverted base profile gate sheet resistance and breakdown voltage are virtually independent.

A thorough investigation of this structure yielded excellent results for GTO's having a wide cathode (>20 mils) and a high gate breakdown voltage (>70 volt)[75-1]. However, the current gain of the NPN section is a rather strong function of the inverted profile. Further, if a low gate turn-off voltage (<30 volts) is one of the (circuit) requirements, the advantage offered by the inverted base concept is largely lost.

Therefore, the uniform base profile of Figure 3-3b emerges as the best compromise and was chosen for the experiments reported on.

The absolute value and importance of a close control of the gate sheet resistance is apparent from the variation of the main electrical characteristics such as the risetime, fall time, and forward voltage drop on this parameter, as is explicit from the data plotted in Figure 3-4[75-1]. A change of ±20% in gate sheet resistance brings about a twofold change for these electrical characteristics, the lifetime in the N-base being kept constant. In particular, the data given in Figure 3-4 apply to a lifetime $\tau_n \sim 1.2$ microseconds and a gate sheet

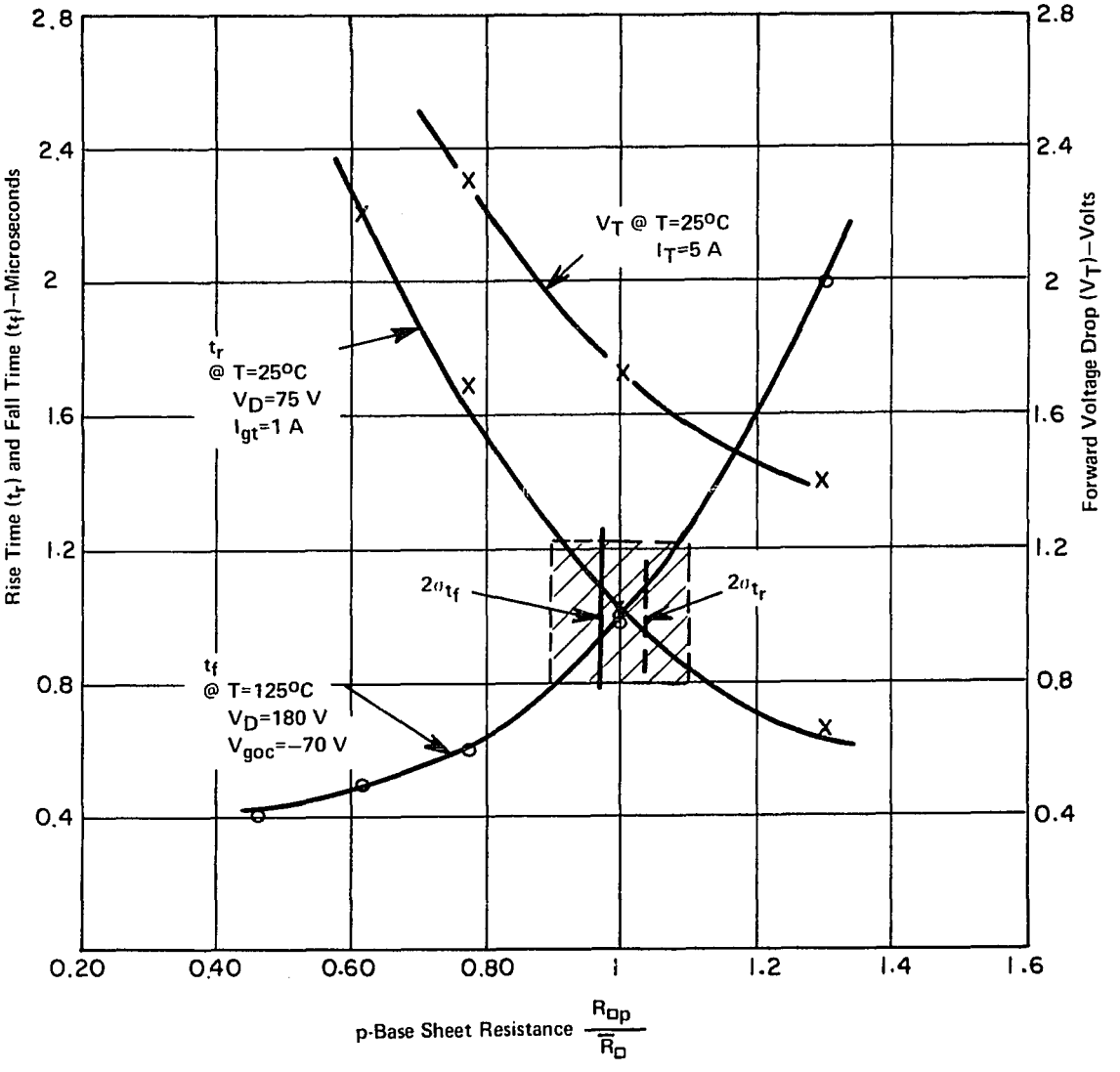

Figure 3-4. Rise Time t_r, Fall Time t_f, and "On" State Voltage vs. Sheet Resistance of (gated) P-Base[75-1]

resistance R_{sp} ~180 ohms/square[1] for $t_{r(25)} = t_{f(125)}$, where $t_{r(25)}$ is the risetime at 25°C and $t_{f(125)}$ is the fall time at 125°C.

2. Minority Carrier Lifetime

The second physical parameter with great influence on the electrical behavior of a GTO is the minority carrier lifetime, specifically the hole lifetime in the wide N-base. In Figure 3-5 we have plotted the rise time t_r, fall time t_f and the forward voltage drop V_T as a function of the average lifetime τ_n in the N-base over a range of 0.8 to 1.4 microseconds, again the gate sheet resistance being kept constant[75-1]. The adjustment of τ_n was achieved by varying the conditions for the gold diffusion[66-2, 72-1, 75-1]. Other means of lifetime control, such as using platinum[75-2, 76-1] or employing electron and gamma irradiation[77-3] were not considered in this study.

It is of course desirable to keep the lifetime low in order to minimize the "tail" in the turn-off phase (see Figure 2-5). However, the lower limit is dictated by the affordable rise time t_r and forward voltage drop V_T. A value for τ_n in the order of 1.0 microsecond, corresponding to a gold diffusion time of 2.0 hours at a temperature of 850°C, appeared to yield a reasonable optimum.

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[1] It should be noted that this represents a deliberate change from usual values. For a "standard" transistor base or thyristor gate R_S is at least an order of magnitude higher, in the range of 1000-10000 ohms/square.

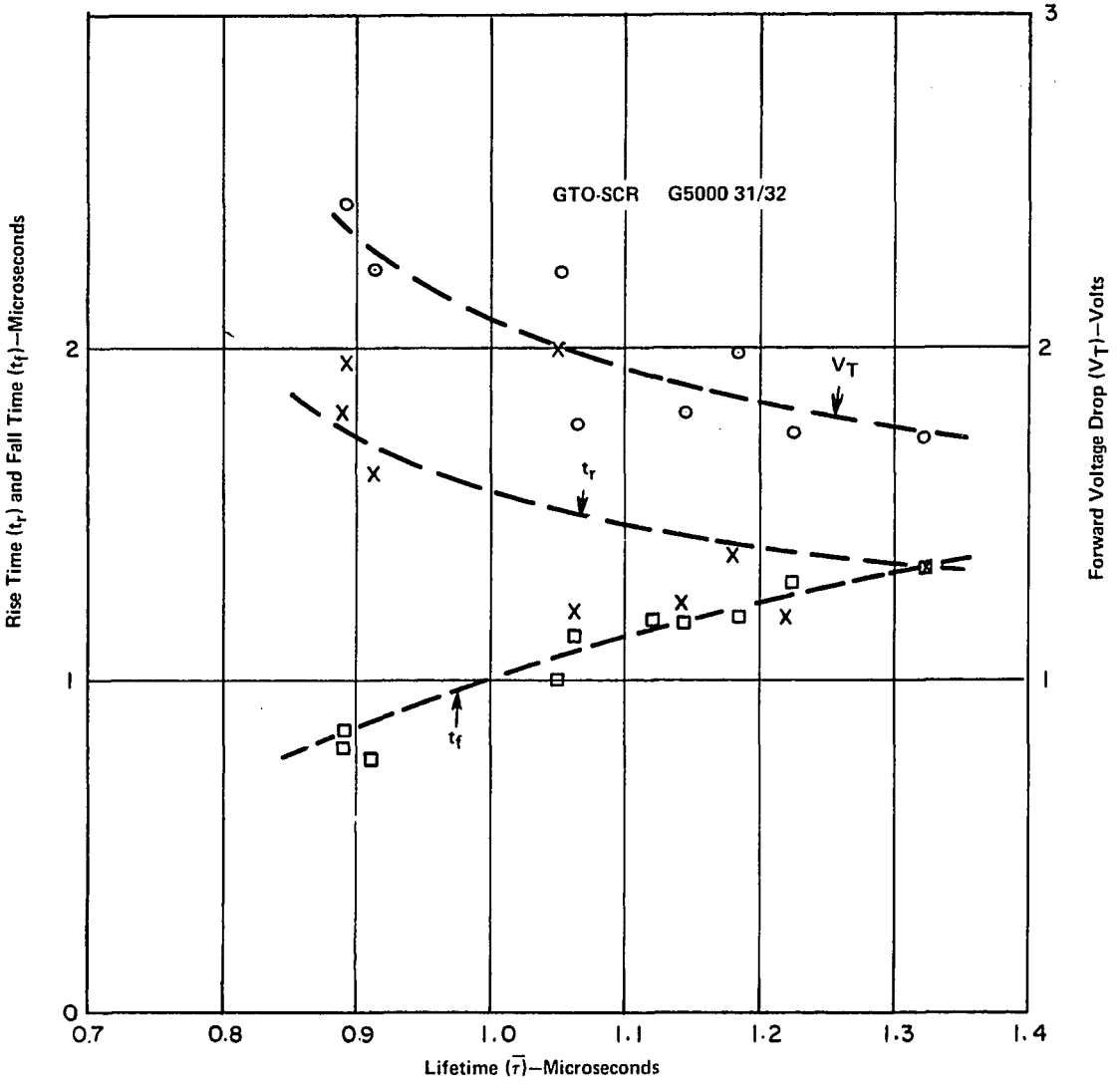


Figure 3-5. Rise Time t_r, Fall Time t_f, and "On" State Voltage vs. Average Lifetime (Au Doping) τ for GTO Thyristor[75-1]

C. Choice of Horizontal Geometry (Interdigitation)

The horizontal geometry was designed with the aim to obtain a meaningful evaluation of the GTO behavior as a function of the lateral turn-off distance L_x (see Figure 2-3a), i.e., the cathode width. For this purpose it would be desirable to fabricate devices with different cathode widths simultaneously on the same wafer. All devices, however, should have the same size, approximately equal total cathode area, and a similar current distribution and heat flow pattern at high current densities. This was accomplished by making use of computer aided mask design procedures[75-4].

In particular, a program was written to create a 3x3 array of test geometrics varying the cathode width over one order of magnitude. The computer program is attached as Appendix A, the test pattern is shown in Figure 3-6[1]. The area of the total array is 456x456 $mils^2$, subdivided into 9 individual devices of 152x152 $mils^2$. The cathode area was kept at about 4000 mil^2; i.e., 15 to 20% of the total area was utilized as cathode. For cathode widths values of 20, 8, 4, and 2 mils were selected. The upper value was predetermined from experiments such that functioning devices (i.e., turn-off) could be obtained with negative gate voltages not exceeding 20 volts for average on-state current

[1] Figure 3-6 is a microphotograph of an array as obtained on a wafer in process, the white areas being the cathode sites opened in the masking oxide. The photomask itself is shown in Appendix B, pp. 147, Mask B-M03.

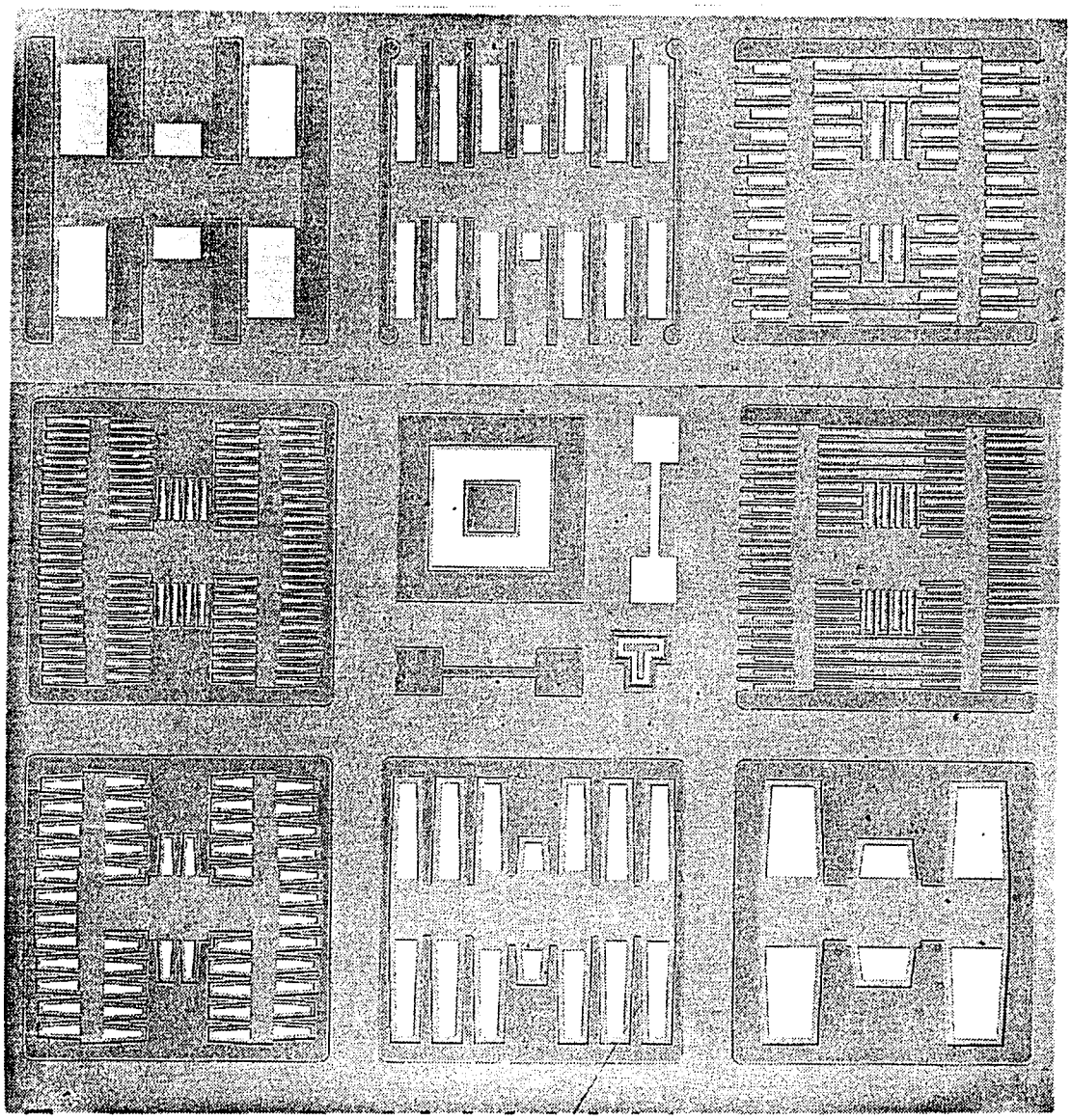


Figure 3-6. Test Array of GTO-Thyristors having Varying Cathode Widths Clockwise from Upper Left: Test Pattern (Rectangular Cathode Sites) 1,2,3,4; Device (Tapered Cathode Fingers) 1,2,3,4

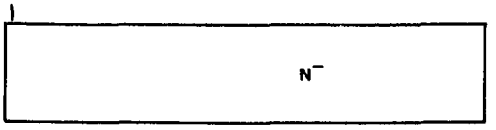
Microphotograph of Section of Actual Device Wafer at "Define Cathode Area" Processing Stage (see Figure 3-7, Step 7, and Appendix B, Mask 03)

densities of about 50A/cm^2 (∿250A/cm^2 cathode current densities). The lower limit of 2 mils was set in order to keep the influence of lateral diffusions and sidewall effects reasonable. As can be seen in Figure 3-6, the 20 mil cathode (Pattern 1) is located in the upper left hand corner, followed clockwise by the 8 mil, 4 mil and 2 mil cathode design, respectively (Pattern 2, 3 and 4). At opposite locations within the array, matching counterparts for each pattern are placed having slightly tapered cathode sites, however (Device 1, 2, 3, and 4). The taper has two functions: a) it lowers voltage drops along the cathode fingers at high currents, b) it will shift the final current filament during turn-off toward the base of the finger in a controlled fashion. This predictable coordinate in the design is a prerequisite for an effective placement of anode shorts (see Figure 1-3) and it is of advantage for implementing the principle of dynamic ballasting as will be discussed in the following chapter.

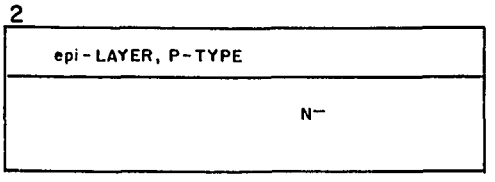
The center pattern serves as a diagnostic device and alignment key.

D. Process for Device Fabrication

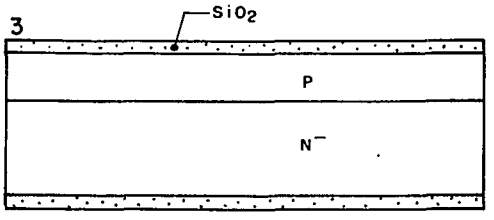
With the vertical structure chosen and the horizontal geometry determined a fabrication process was developed, the basic steps of which are outlined in Figure 3-7 on the following three pages. Figure 3-7 should be largely self-explanatory. The process contains several special features which are not found in a conventional device fabrication, however. In step 2 a low resistivity P-type layer is epitaxially grown



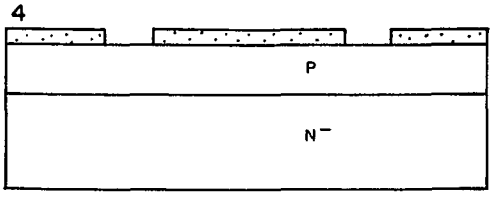
Starting Material, Si <III> axis
$25 < \varrho < 45\ \Omega cm$, ~ 9 mil thick



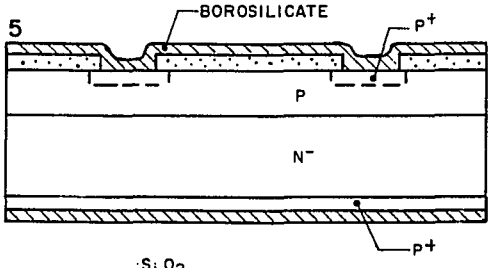
Grow epitaxial gate layer; 0.25 Ωcm
1.2 mil - grind and etch backside
to total thickness of 7.2 mils



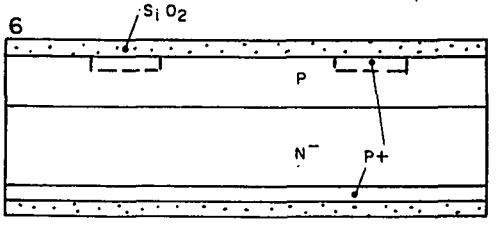
Grow initial oxide, 12000 Å -
6 hrs. @ 1000 °C



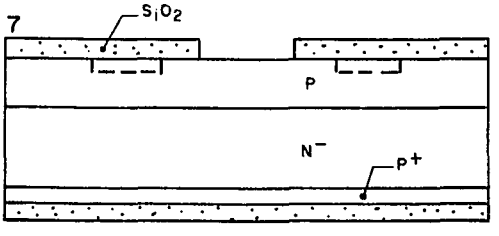
Define P+ gate-contact areas by
photolithography (see B-Mask 01)



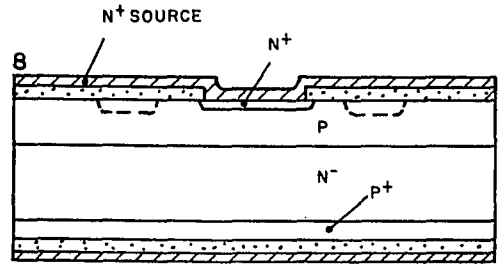
Deposit Boron diffusion source,
diffuse 1 hr. @ 1225 °C -
form anode and gate-contact layer



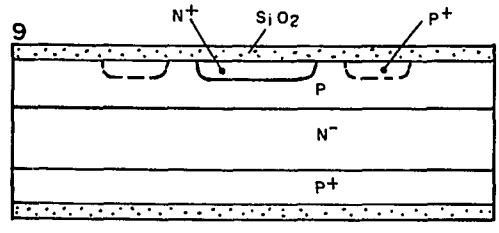
Strip Boron glass and oxide,
regrow new oxide, 12000 Å
6 hrs. @ 1000 °C



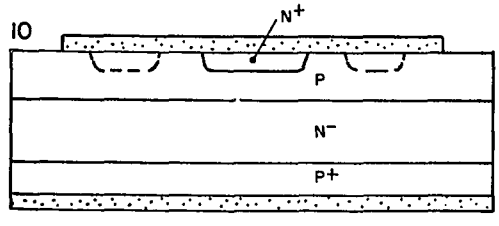
Define cathode areas in oxide
photolithographically (B-Mask 03)



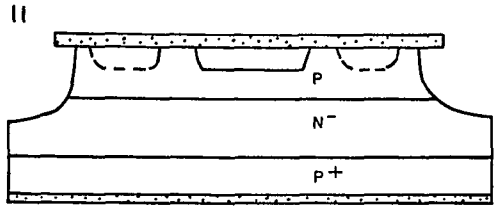
Deposit N+ Cathode from $POCl_3$ source, - 5-15-20 min. @ 1200°C



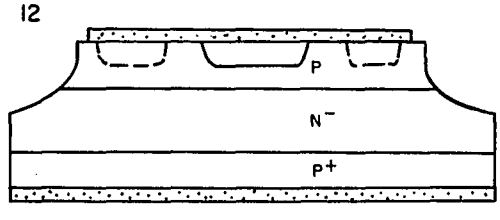
Etch off phosphosilicate and $Si O_2$ - Drive in Boron and Phosphorus at 1265°C for 30 min. with simultaneous growth of final oxide; slow cool to 800°C @ 3°C/min.



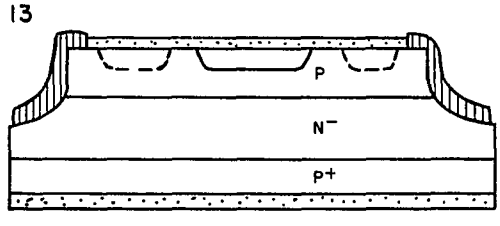
Define Mesa grid in oxide (see B-Mask 06)



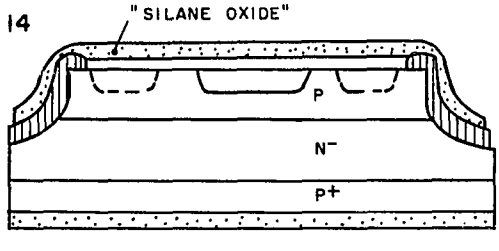
Etch Mesa about 3 mils deep using $HF\text{-}HNO_3$. Individual devices with plane forward blocking junction are formed.



Remove oxide overhang (B-Mask 08)

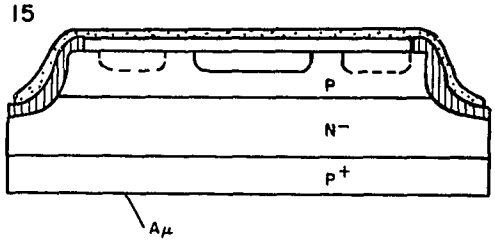


Apply glass frit (IP820), fire and anneal glass in special two-zone furnace. Junction J_2 is now passivated.



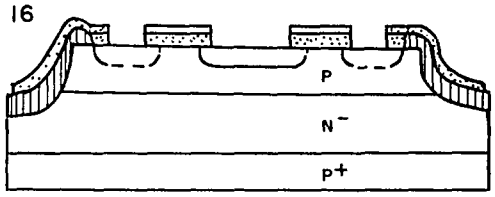
Deposit protective low temperature oxide, synthesized from $Si H_4$ and O_2, over wafer top, ~8000 Å

15



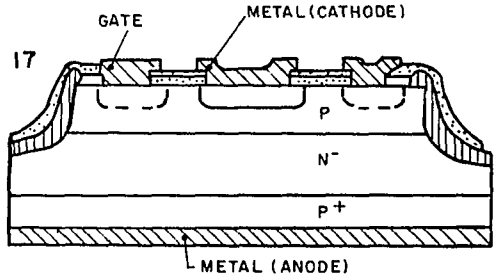
Etch bottom oxide off, plate Gold on backside, diffuse in two-zone furnace using special conditions - $\bar{\tau} \sim 1.0\ \mu s$

16



Define cathode and gate contact areas in oxide (B-Mask 04)

17



Evaporate trimetal (Al-Ti-N_i), define contact pattern (B-Mask 07, inverse) sinter metal for 20 min. @ 425 °C

18

Separate devices by laser scribing; test dice

19

Assemble units on TO-3 stem, RTV coat and seal. Final stabilization bake: 24 hrs. @ 150°C.

Figure 3-7. Basic Process Outline for Fabrication of High Speed, Epi Base GTO-Thyristor (3 pages)

on a high resistivity N-type substrate. The sequence 13 to 15 shows a junction glass passivation compatible with a subsequent gold diffusion.

A typical resistivity profile along a cross section through a finished device (through the center of the device structure at step 16, or 17 with metal removed) is given in Figure 3-8. This profile was obtained by angle lapping a sample and taking two point probe - spreading resistance measurements[74-2, 79-4]. We see the cathode layer w_k on the left, having a very low resistivity of 5×10^{-3} Ωcm, the junction x_{j2} being located 11 microns from the top surface. The anode layer w_A is seen on the right hand side, the junction x_{j3} being located 24 microns from the bottom surface. The forward blocking junction x_{j2} separates the low resistivity gate layer (w_G = 19 micron, $\rho_{min.}$ = 0.28 Ωcm) from the high resistivity N base (w_N = 126 micron, $\bar{\rho}$ = 36 Ωcm) which is the leftover portion of the initial substrate and is supporting the high breakdown voltage.

E. Results

Devices were fabricated in accordance with the process described in the previous section, and they were subjected to an extensive electrical evaluation.

In general, a distinct difference in behavior of devices having either parallel cathodes or tapered cathodes could not be established because of overlapping distributions for the various electrical parameters. Therefore, data and results presented in this section are applicable to both versions.

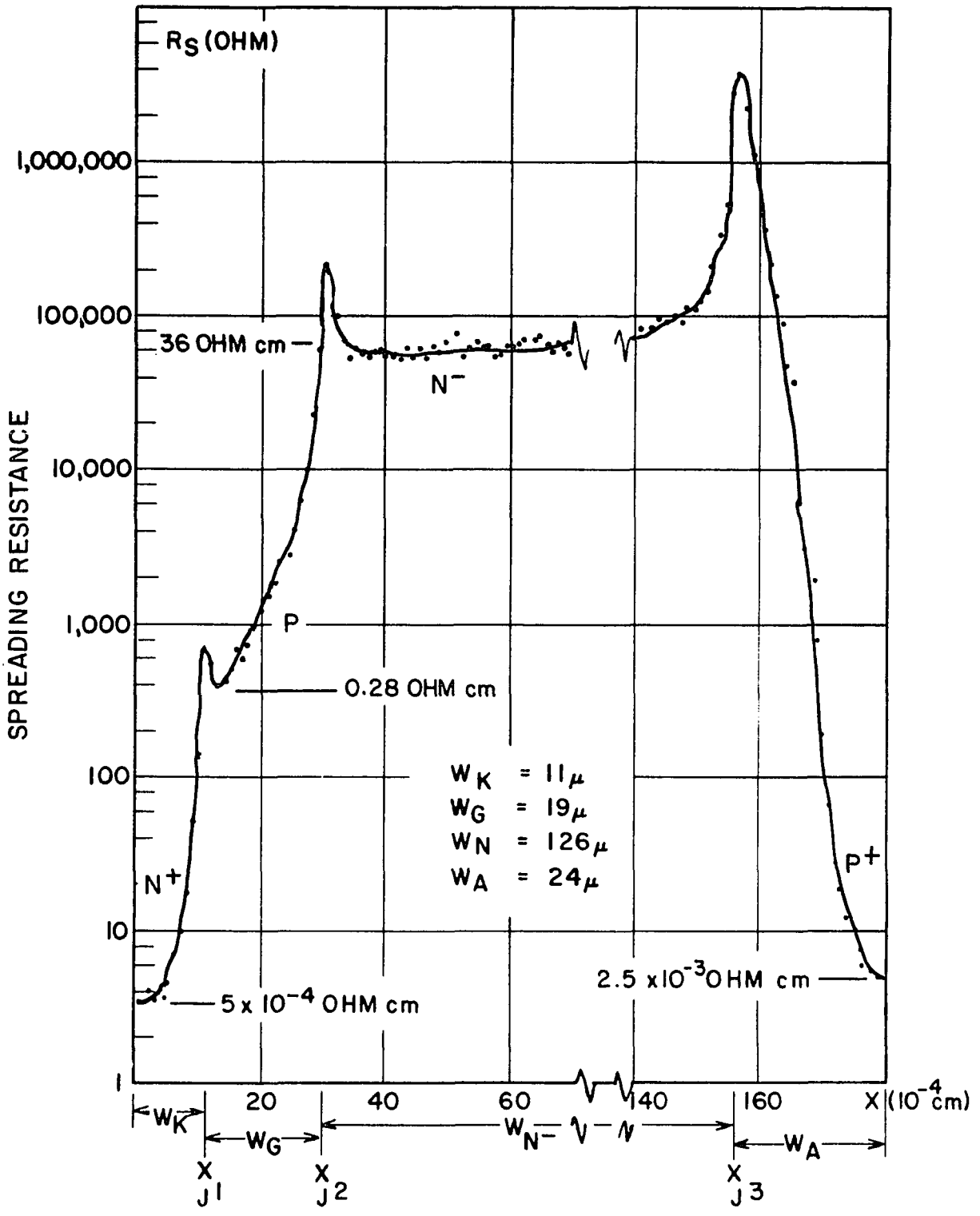


Figure 3-8. Two-Point Probe - Spreading Resistance Profile for High Frequency-Epi Base Structure

1. Static Data

Results of static data for one typical set of devices are given in Table 3-1. These devices come from the same wafer and were selected from the lower side of the I_{gt} and V_T distribution.

As can be seen the forward blocking voltage V_{DRXM} lies between 600 and 700 volts and is geometry independent. This value is surface-contour limited below the actual bulk breakdown. The gate-cathode breakdown voltage V_{GK} of approximately 21 volts is also independent of geometry and is consistent for a planar junction with a profile as shown around x_{j1} in Figure 3-8. The forward voltage drop V_T and the gate trigger current are strongly dependent on cathode width. The variation of cathode area from device 1 to 4 is less than ±20%, and the increase in V_T from 1.8 volt for the 20 mil cathode to 3.4 volts for the 2 mil cathode may point toward a somewhat non-uniform current distribution. This fact is contradicted by the increase in gate trigger current which is roughly proportional to the periphery indicating a reasonable uniform turn-on, which certainly points toward uniform conduction in the steady-state condition. The increase in V_T with decreasing cathode width can be explained if one takes into account the gettering effect of the phosphorus cathode layer on the gold concentration[72-1] in the active gate region.

The wide cathode will more effectively getter toward the center of the cathode and establish a relatively uniform lifetime $\bar{\tau}$ beneath the cathode.

Device Type	$W_{Cath.}$ (mils)	V_{DRXM} (V)	V_{GK} (V)	V_T (V)	I_{gt} (mA)
1	20	600	21.0	1.84	6.8
2	8	656	20.7	2.07	25.6
3	4	623	20.4	2.40	53.2
4	2	661	21.2	3.38	167.5
Conditions for		0.2 mA I_{RXM}	0.2 mA I_{RGK}	10 A I_T	12 V V_A

Table 3-1. Static Data for GTO Thyristor with Varying Cathode Width

The narrow cathode will be more dominated by edge effects, i.e., less gettering is experienced. Hence, a lower average lifetime $\bar{\tau}$ is achieved leading to a shorter diffusion length and consequently to a higher forward voltage. This effect may be enhanced because of sidewall injection resulting in a higher average gate width $\bar{w}_G$ reducing the effective transport factor even more.

2. Major Test Conditions

Switching characteristics were determined using a pulsed anode supply and a resistive load. The input-output wave forms are schematically given in Figure 3-9.

A turn-on pulse of 1 ampere with a 50 nanosecond rise time and an approximately 10 microsecond duration was applied to the gate. A negative turn-off pulse was applied from a voltage source about 50 microseconds later. Generally, an inductance was put in series with the input. The time duty cycle was kept below 2.5% in order to avoid internal device heating. All data presented were taken with an anode supply voltage V_{DD} of 200 volts, and without a snubber network or a voltage clamp across the output of the device under test.

3. Turn-On

The turn-on characteristics are shown in Figure 3-10. The delay time t_d is less than 50 nanoseconds and the rise time is about 500 and 400 nanoseconds, for 25°C (Figure 3-10a) and 125°C (Figure 3-10b), respectively.

The surprising feature is that there is virtually no dependence of rise time t_r on cathode width. One would expect that device 1 with a 20 mil wide cathode exhibits the longest t_r. However, quite contrary, the

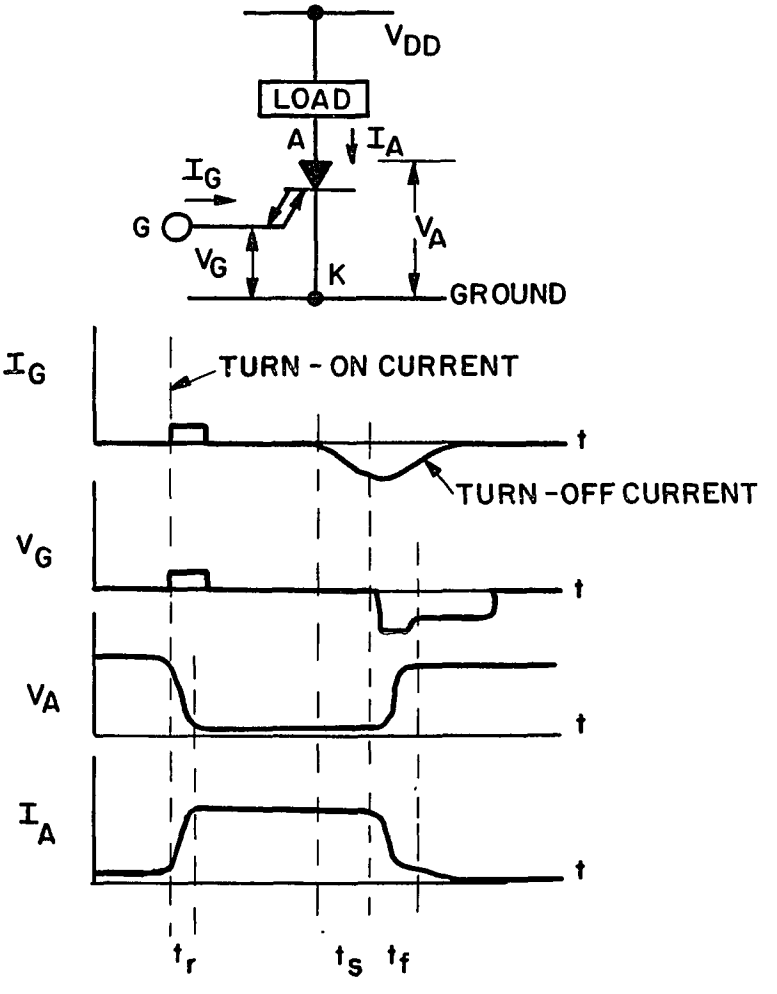


Figure 3-9. Input-Output Waveforms for GTO Thyristor in Anode Load Configuration

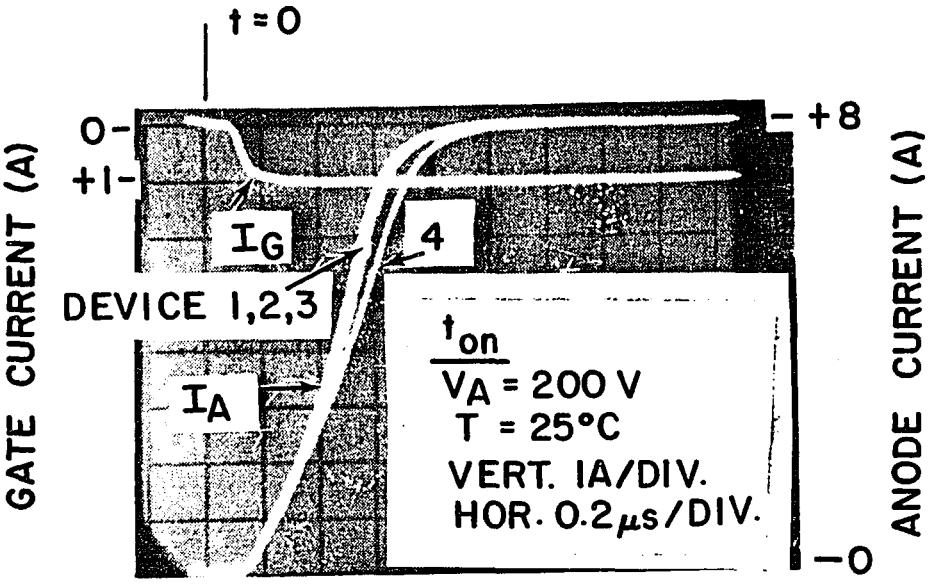


Figure 3-10a. Gate Turn-On Current $I_{GT} = f(t)$
Anode Load Current Response $I_A = f(t)$

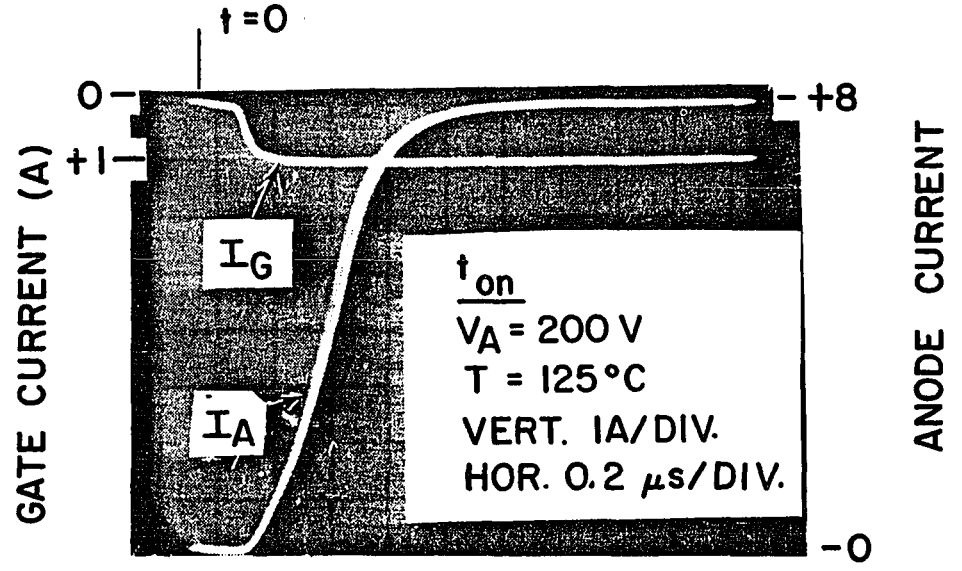


Figure 3-10b. [I_{GT}, I_A] = f(t)

Figure 3-10. Turn-On Characteristic of High-Frequency GTO-Thyristor at 25 °C and 125 °C Device 1, 2, 3, and 4

trend is actually reversed. Device 4 with a 2 mil cathode width has the longest rise time as evident from the traces in Figure 3-10a.

The reason for this must be a differing spreading velocity in the individual devices. Since the spreading velocity is proportional to the square root of the lifetime, $v_s \propto \sqrt{\tau}$ [63-1, 73-1, 75-3] we may conclude that the lifetime beneath the active gate decreases with decreasing cathode width. This fact is consistent with the observations made about the variations in forward voltage drop V_T in Section 3, thus confirming a more pronounced gettering of gold under the wider cathodes.

Lastly, we notice in Figure 3-10 that the turn-on condition for an output current I_A = 8A and for the duration of the input pulse represents the equivalent of a forced current gain h_{FE} = 8, h_{FE} being the DC-current gain, as is customarily defined for transistors.

4. Turn-Off Characteristics (General Waveforms)

The turn-off waveforms are shown in Figure 3-11. These waveforms represent a typical example of the input-output relationship for currents and voltages as a function of time during the turn-off phase.

In Figure 3-11a we see the negative gate current $I_{gq}(t)$ and the corresponding anode current response $I_A(t)$ at the gate terminal and anode terminal, respectively. The coinciding input voltage $V_{gq}(t)$ and the output voltage response $V_A(t)$ are traced in Figure 3-11b. The application of the turn-off pulse, t=0, occurs at the first vertical grid line on the left hand side of the display.

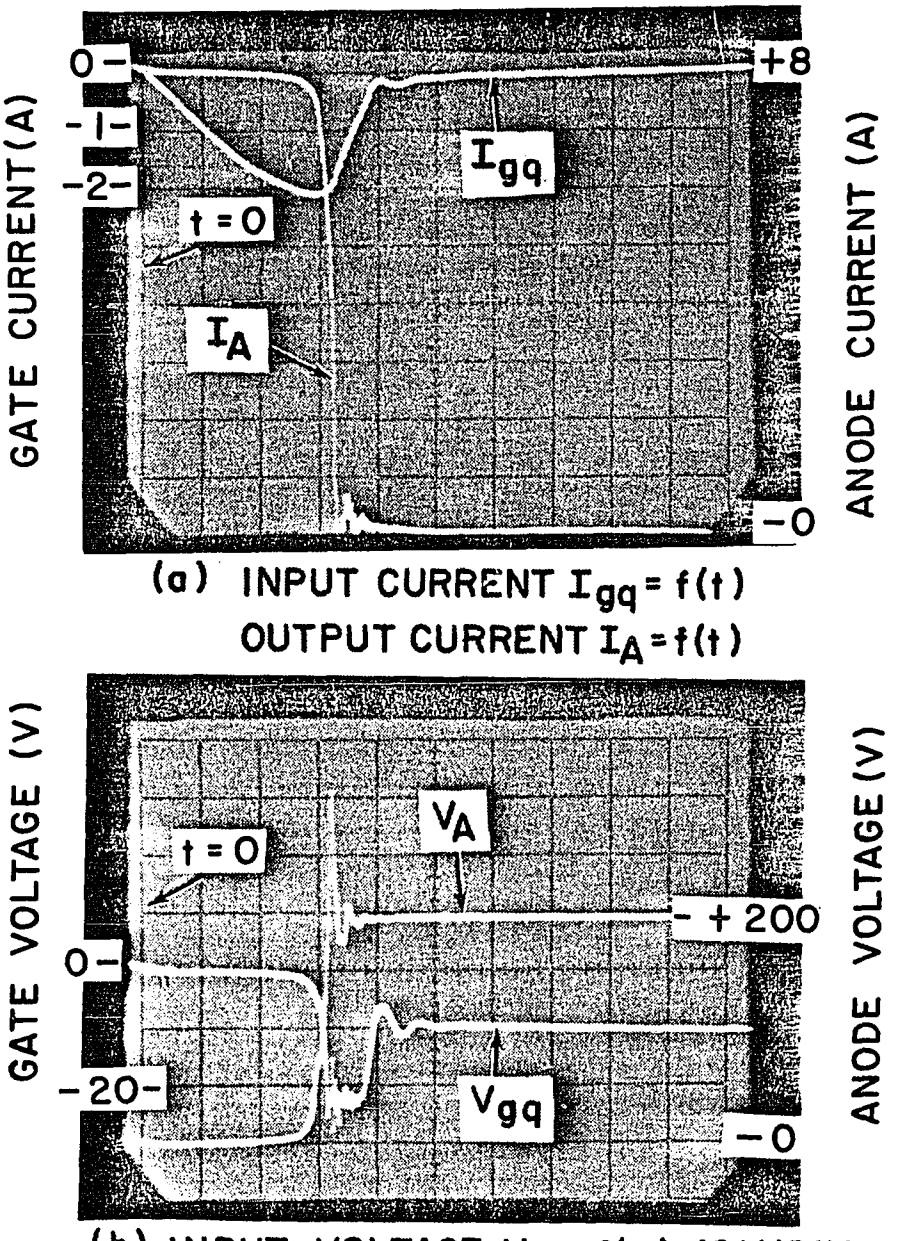


Figure 3-11. Turn-Off Characteristics for High-Frequency GTO-Thyristor (Example of Waveforms)

The gate current I_{gq} rises approximately linear during the whole storage phase t_s ($\sim$1.4 microseconds), while the anode current remains constant (I_A = 8A). The slope of the gate current is mainly a function of the gate series inductance L_{gs} ($\sim$4.6μH) and the open circuit-gate source voltage V_{goc} (-10V). The maximum gate current $I_{gq\ max}$ ($\sim$2A) is reached after the storage phase is completed and the anode current is in the fall period just before the current traces intersect each other (Figure 11a).

At that point the cathode junction is reverse biased and has assumed the gate source voltage V_{goc} (-10V); the voltage across the inductance being zero.

The fall of the anode current I_A is now aided by the reversal of the polarity at the gate inductance L_{gs}, and the additional negative turn-off voltage which is developed at the gate (Figure 11b), while the stored energy in L_{gs} is being discharged. Actually, it may be noticed that the gate cathode junction is driven into breakdown acting as a voltage clamp for approximately 0.3 microseconds. During this period the negative gate current I_{gq} decreases to zero with a slope determined by L_{gs} and the gate breakdown voltage V_{Gbr} ($\sim$22V) and then the gate voltage assumes the open-circuit value V_{goc} = -10V. The small tail of anode current decays simultaneously and the center junction J_2 recovers and becomes reverse biased. Thus, the anode voltage V_A assumes the supply voltage V_D = 200V. The overshoot of about 100 volts and the ringing is a consequence of some lead inductance in the load circuit, interacting with the device

output capacitance. Since the maximum value of the transient voltage remained well below the actual junction breakdown of J_2, no efforts were made to reduce this parasitic inductance for the measurements presented here.

5. The Influence of the Gate Series Inductance

An inductance in series with the gate proved to be an important element for safely operating a GTO. In Figure 3-12 we see the turn-off characteristics for a device type 3 (4 mil cathode). Curve 1 shows the gate current and anode current without an inductance connected between the gate and the voltage source. For curve 2 and 3 an inductance of 4.6 microhenry and 11.8 microhenry were inserted, respectively. The open circuit gate voltage was $V_{goc} = -15$ volts in all cases.

As can be seen in curve 1 the storage time t_s lasts about 0.5μs and the fall time t_f only 0.1μs. The peak gate current $I_{gq\ max}$ reaches 4 amperes, i.e., the turn-off gain $G_{gq} = 2$. Further, as the (average) anode current I_A reaches the break at approximately 3% of the On-state current, the negative gate current breaks also. The "tail" current in the anode is identical to the gate current, the decay time being about 0.5μs. This is a situation as described in Chapter II and shown in Figure 2-5. At the break, the cathode has shut off and is reverse biased, the negative voltage being smaller than the gate-cathode junction breakdown voltage.

For the curves 2 and 3 the storage time t_s increases while the peak gate current $I_{gq\ max}$ decreases. The falltime, however, is at least as

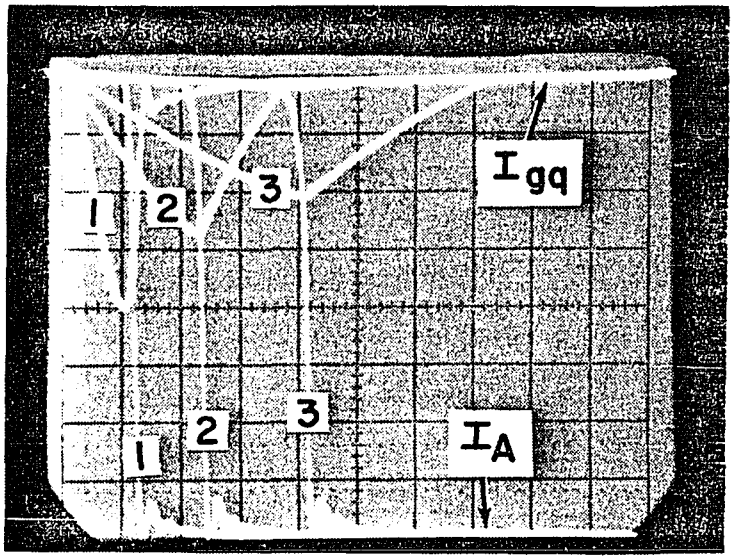


Figure 3-12. Turn-Off for GTO-Thyristor [I_A, I_{gq}] = f(t) with Gate Series Inductance L_{gs} as Parameter Device Type 3 (4-mil Cathode)

fast as in the case for curve 1, i.e., t_f=0.1μs. The break and tail for the anode current I_A remain relatively unchanged.

The significant difference is in the waveform of the gate current, the magnitude of which stays always above the anode tail current. This fact indicates that cathode current flows in the reverse direction, the entire gate-cathode junction J_1 is in avalanche breakdown (as shown in Figure 3-11b before) and the GTO stays safely turned off.

It must be emphasized here that the snap into breakdown by means of an inductive kick is rather different from the local edge breakdown caused by the lateral voltage drop due to I_{gq} flowing through the resistive gate region beneath the cathode.

In the first case the electron-hole plasma is being rapidly extinguished once it has been squeezed into a filament during the storage phase as evidenced from the negative potential built-up across the gate-cathode terminal (see Figure 3-11b).

In the latter case the electron-hole plasma keeps flowing in a partially squeezed condition and a negative potential is never developed across the gate-cathode terminal because the center section of the cathode junction remains forward biased (see Figure 1-2c, pp. 8). Thus, a hot spot forms and eventual device failure results due to local burnout.

Turning our attention now to the peak reverse gate current, for instance for curve 3, we notice that this value is now 2 amperes rather than 4 amperes as for curve 1. The turn-off gain is here increased to

G_{gq} = 4, while the internal lateral voltage drop is kept to one-half of that developed in case 1. Also, the negative gate bias is equal to the highest possible voltage, namely the cathode breakdown voltage V_{Gbr} = -23V, while the open circuit drive voltage, V_{goc} = -15V, can be considerably lower.

It is obvious that it would be much more difficult to achieve turn-off if the maximum gate current would be limited through an added external resistance. The turn-off voltage available would be much lower than the open circuit voltage at the critical point where the current density in the device has reached a local maximum. In addition, a portion of the turn-off energy delivered by the gate drive source is needlessly dissipated in the series resistor.

The above discussion leads to the following summary about the influence of a gate series inductance for turn-off of a GTO:

a. an increased turn-off gain can be obtained,

b. lower lateral internal voltage drops are encountered,

c. the applied source voltage can be lower and is not as critical, and

d. an increase in storage time must be tolerated.

In general, with the application of a gate series inductance a safe turn-off condition can be maintained, and as an indirect benefit a smaller device may be employed for generating the drive function to achieve turn-off.

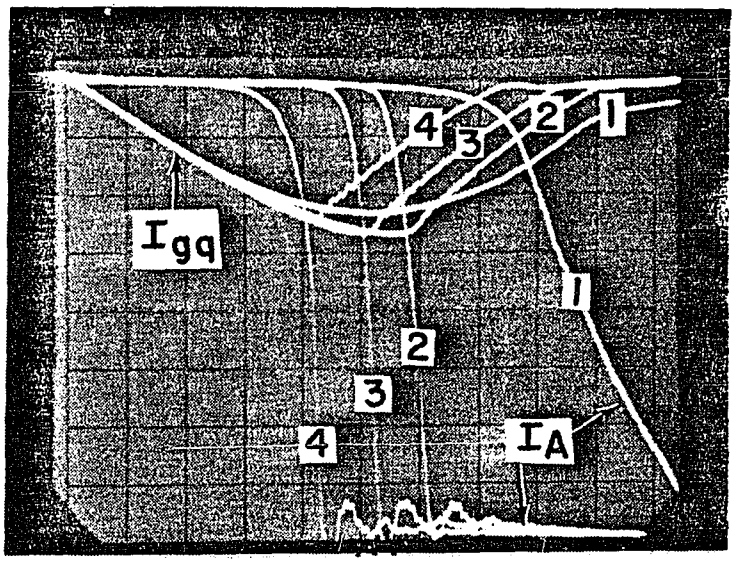
6. Dependence on Cathode Width

The effect of the cathode width on the turn-off behavior of a GTO is of great interest. Figure 3-13 depicts the input current-output current time response of devices with a 20 mil, 8 mil, 4 mil, and 2 mil wide cathode, curves 1, 2, 3, and 4, respectively.

The input circuit and the drive condition as well as the output supply voltage and load resistance were kept constant (L_{gs} = 4.6μH, V_{goc} = -15V, V_D = 200V, $R_L \sim 25\Omega$).

We observe that the storage time t_s and the fall time t_f are pronounced functions of the cathode width. The storage time increases from 0.7 microseconds for the 2.0 mil cathode (curves 4) to 1.5 microseconds for the 20 mil cathode (curves 1). The fall time changes from approximately 0.1 microseconds for the 2 mil cathode to 0.6 microseconds for the 20 mil cathode. The turn-off gain remains relatively unchanged.

These results differ from previously published data by Kao and Brewster[74-3] who report that both storage time t_s and turnoff time ($t_s + t_f$) "were much the same and did not depend on cathode width". Their case, therefore, implies that one-dimensional conditions existed, i.e., the cathode width $L_x < 2L_n$. This would require a minimum lifetime $\overline{\tau}_p \sim 50$ microseconds for the maximum cathode width of 25 mils that was used in Reference 74-3. Such a long lifetime causes a large recombination tail (see Figure 2-5, pp. 28). Consequently, this



CATHODE WIDTH

1 = 20 MIL 3 = 4 MIL
2 = 8 MIL 4 = 2 MIL

t = 0.2 μs/DIV. T = 25°C
I = 1A/DIV. V_{goc} = -15 V
Lgs = 4.6 μH

Figure 3-13. Turn-Off Behavior of GTO-Thyristor with varying Cathode Width [I_A, I_{gq}] = f(t) $W_k = L_x$ as Parameter

device would suffer from excessive switching dissipation and be vulnerable to retriggering. These conditions can only be remedied by adding a polarized snubber network in parallel to the anode[75-4, 77-4], and high speed operation and circuit efficiency are greatly impaired, however.

7. Turn-Off Criteria and Current Densities

Considering the waveforms obtained in this work for varying cathode width some important turn-off criteria may be established.

Examining the I_A-traces depicted in Figure 3-13 during the fall period we detect that for devices 2, 3, and 4 the slope dI_A/dt increases up to the tail break point. Also, the maximum gate current is reached only after the anode current has substantially decreased.

That does not hold for Device 1. Here the slope of I_A goes through an inflection at about 4A decreasing with time, i.e., the second derivative of anode current with respect to time d^2I_A/dt^2 becomes negative. Also, the gate current displays a broad maximum and peaks long before the anode current is intersected. From such a waveform we may infer that in this case for the 20 mil wide cathode the lateral base resistance gains dominance toward the end of the storage phase. Thus, the gate source voltage is marginal for turn-off and a pronounced inductive voltage spike as for instance seen in Figure 3-11b is absent. A slight decrease in turn-off voltages or increase in temperature will cause failure to turn-off.

The difference between safe turn-off and potential turn-off failure becomes rather clear if we plot the ratio of anode current to gate current dI_A/dI_{gq} against time during the turn-off phase as is shown in Figure 3-14 using the waveshapes of Figure 3-13.

Without a gate series inductance turn-off, i.e., the storage phase, will commence with infinity at t = 0, where the gate current is $I_{gq} = 0$ and the anode current $I_A = I_T$, and then monotonically decrease to unity at the tail break, from which point anode current and gate current are identical (see Figure 2-5 and 3-12 trace 1).

With the gate series inductance the differential turn-off gain dI_A/dI_{gq} behaves similar from t = 0 throughout the storage phase and fall phase. But at the tail break the differential turn-off gain is now much less than unity and it approaches unity for $I_A \rightarrow 0$ and $I_{gq} \rightarrow 0$ in an asymtotic fashion. This behavior constitutes a safe turn-off condition as is exhibited by devices 2, 3, and 4 (8, 4, and 2 mil cathode).

In contrast for device 1 (20 mil cathode) the differential turn-off gain never reaches unity during the fall time but rather shows an increase of dI_A/dI_{gq} toward the end of the fall time signaling instability. The peak will grow or move out in time with either a slight increase in local temperature or decrease in gate source voltage and eventually cause turn-off failure as mentioned above.

The inserted table in Figure 3-14 gives the "conventional" turn-off gain G_{gq}, the ratio of the on-state current I_T to the maximum negative gate current $I_{gq\ max}$, during turn-off. As should be noted G_{gq} is identical for device 1 and device 4, and it is clearly demonstrated by the given example that the use of this electrical parameter in the literature may lead to erroneous conclusions unless additional information is provided.

The danger of destruction existing for a GTO is evident from 1st order estimates of current densities which may develop locally during turn-off. Table 3-2 shows the (worst case) peak current densities for the four geometries investigated in this study. The assumptions for the given values of $J_{o(max)}$ are that the total on-state current $I_T = 8A$ is flowing through an area of width $2L_n$, and the lifetime τ beneath the cathode is of the order of 1 microsecond.

One sees immediately that for a uniform line turn-off over the length of the cathode sites "reasonable" conditions exist (two-dimensional case: $J_{o(max)2d}$ ranging from 462 A/cm^2 to 3340 A/cm^2). Unfortunately, these lines will not stay uniform, but rather degenerate to spots having a diameter of $2L_n$. Therefore, extreme conditions are highly probable (three-dimensional case: $J_{o(max)3d}$ ranging from 5000 A/cm^2 to 87000 A/cm^2!). Though counteracting mechanism tends to limit J_o, i.e., Auger effects and bandgap narrowing, the necessity of narrow cathodes and careful design of turn-off circuits becomes rather explicit.

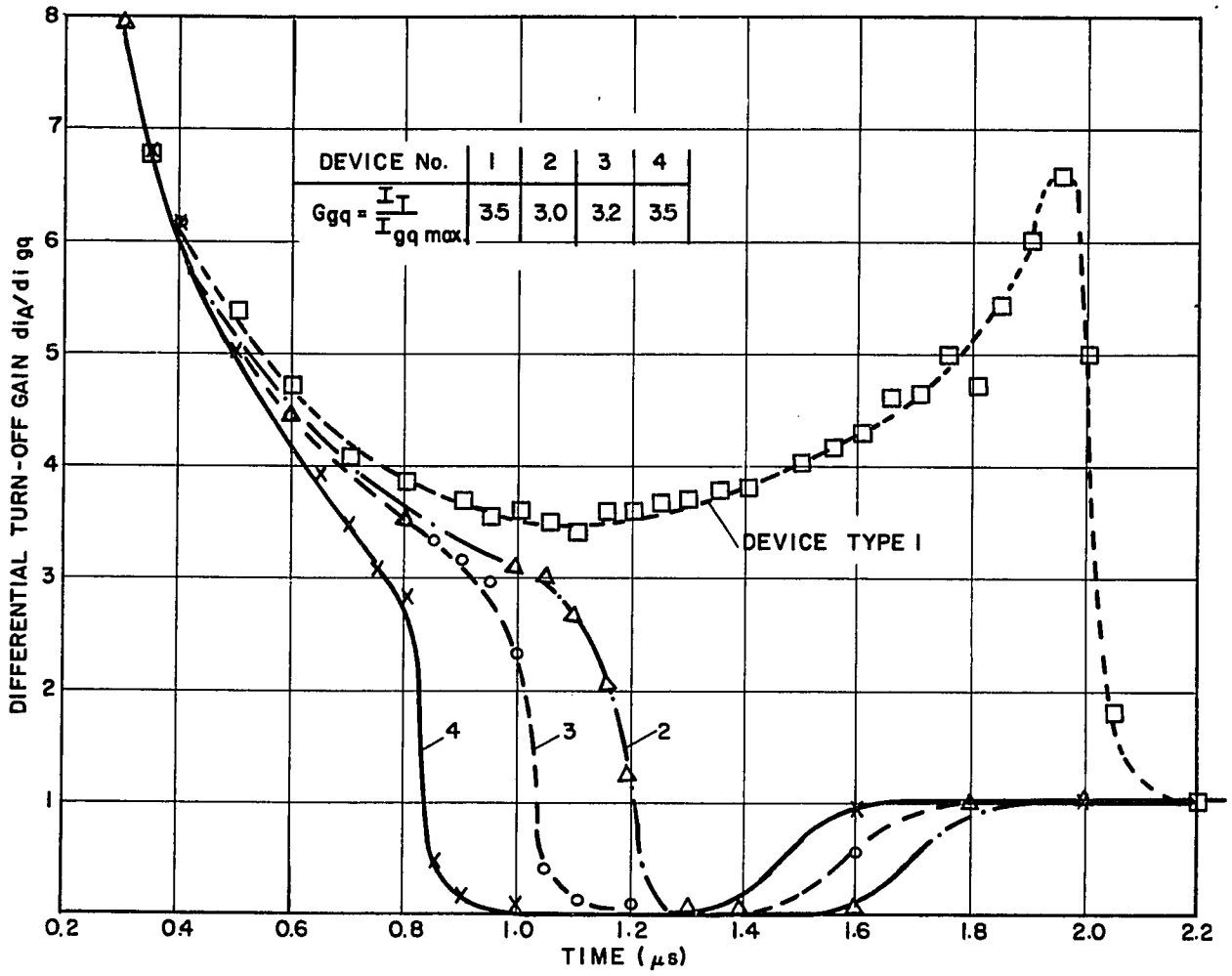


Figure 3-14.
Differential Turn-Off Gain (di_A/di_{gq}) vs. Time for GTO Thyristors having different Cathode Widths under Identical Input and Output Conditions; showing safe Turn-Off for Device Types 2, 3, 4 (2, 4 and 8 mil cathode, respectively), and indicating Onset of Turn-Off Failure for Device Type 1 (20 mil Cathode). V_D=200 V, I_T=8 A, V_{goc}=-15 V, L_{gs}=4.6 μH, T=25° C (for I_A, I_{gq}=f(t), See Figure 3-13

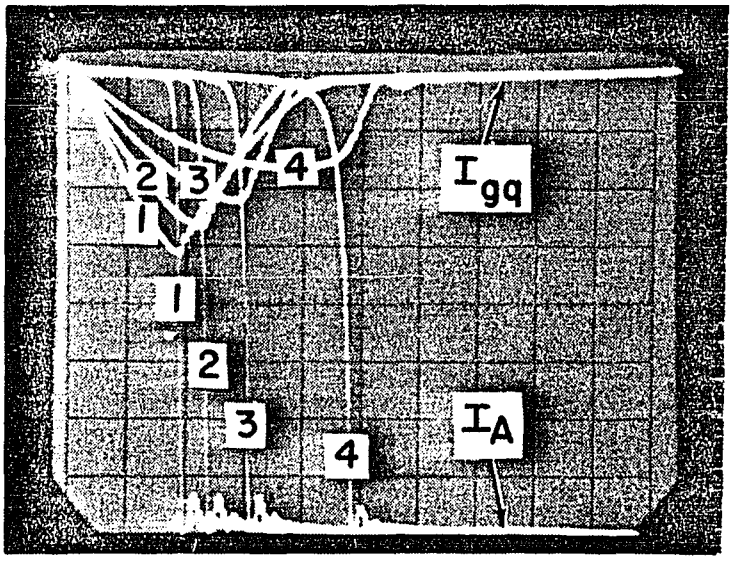
8. Influence of Negative Gate Bias and Temperature

Figure 3-15 shows the turn-off characteristic of Device 3 (4 mil cathode) for varying open-circuit gate voltages V_{goc} = -20V, -15V, -10V, and -5V, respectively, at 250°C. The gate series inductance L_{gs} = 4.6 microhenry, the anode supply voltage V_D = 200V.

While curves 1, 2, and 3 (V_{goc} = -20V, -15V, and -10V) show that turn-off is input circuit dominated, we see that for curves 4 (V_{goc} = -5V) lateral series resistance and continuing current injection start to become dominant. However, even though the storage phase becomes significant (t_s > 2μs) and the fall time starts to increase noticably (t_s ∿ 0.3μ), the criteria for safe turn-off as defined in Section 7 are still met.

In Figure 3-16 we see the temperature dependence of the same device in the range from 25°C (curves 1) to 125°C (curves 4). The time scale is here expanded to 0.2μs/Div, L_{gs} = 4.6μH, and V_{goc} = -15V.

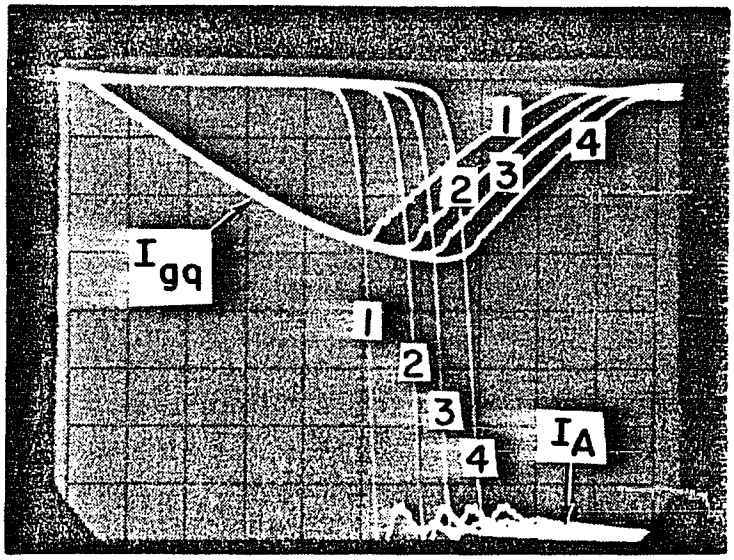
The turn-off at 125°C is excellent. Generally, the behavior is as would be expected, i.e., storage time, fall time, and tail contribution increase with temperature consistent with a lifetime increase. The slope of the gate current during the tail phase increases because the gate breakdown voltage V_{Gbr} becomes larger due to changes in avalanche multiplication. A very qualified statement can be made for the decrease in turn-off gain G_{gq}. With increasing temperature the α's of the component transistor sections become larger. Therefore, it becomes harder



NEGATIVE GATE BIAS (V_{goc})

1 = -20V 2 = -15V 3 = -10V 4 = -5V
t = 0.5 μs / DIV. T = 25 °C I = 1A / DIV.

Figure 3-15.
Turn-Off Behavior of GTO-Thyristor for Varying Negative Gate Bias [I_A, I_{gq}]=f(t), V_{goc} Parameter Device Type 3 (4-mil Cathode)



TEMPERATURE

1 = 25°C 2 = 65°C 3 = 95°C 4 = 125°C

t = 0.2 μs / DIV. I = 1A / DIV.

Figure 3-16.
Turn-Off for GTO-Thyristor dependent on Temperature [I_A, I_{gq}]=f(t), T Parameter Device Type 3 (4-mil Cathode)

to force the condition for the loop gain G_L to be less than unity everywhere over the entire device area (see Equation 1-3, pg. 6).

Of interest in the characterization of the GTO turn-off behavior is to see how the gate source voltage effects the fall time for the various geometries, because the switching dissipation is largely determined by this parameter. The fall time t_f is plotted as a function of the negative gate source voltage at 125°C for Device Types 3, 2, and 4. The devices with the 4 mil and 8 mil cathode width could not safely be operated for $V_{goc} < 10V$. Considering the results plotted in this graph and the forward voltage drop V_T (see Table 3-1, pp. 62) Device Type 3, operated at $V_{goc} = -15V$, appears to be a proper choice to achieve optimum performance.

9. Turn-Off For Varying Loads

Figure 3-18 shows the turn-off characteristics of Device 3 for varying anode loads at 125°C. The load resistance was changed over a range from $R_L \sim 100\Omega$ ($I_T = 2A$) to $R_L \sim 16.7\Omega$ ($I_T = 12A$). The anode supply voltage $V_D = 200V$, and the input drive conditions ($V_{goc} = -15V$, $L_{gs} = 4.6\mu H$) were kept constant. The current scale is in this case 2A/Div.

Curves 1 show a circuit determined (forced) current gain ($I_T/I_{gq\ max}$) of unity. Both, turn-off gain and storage time increase with increasing current. The turn-off gain at $I_T = 12A$ is approximately 3.3. At that point, turn-off is still well behaved to assure safe operation. It may be also noticed that the fall time is relatively independent of anode

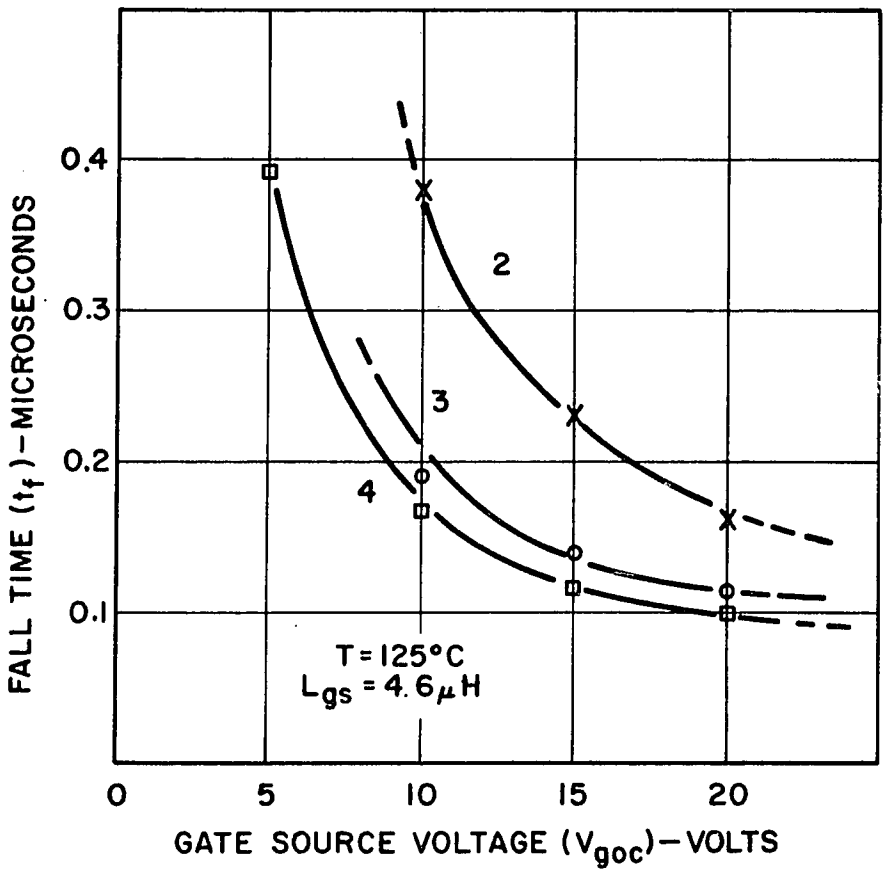
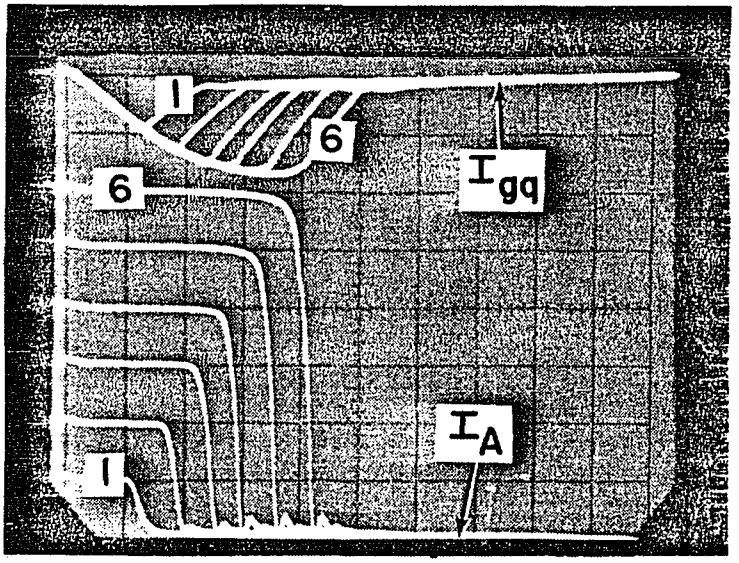


Figure 3-17.
Fall Time for GTO-Thyristor as Function of (Open Circuit) Gate-Source Voltage $t_f = f(V_{goc})$, $W_k = L_x$ as Parameter
2=Device Type 2 (8-mil Cathode)
3=Device Type 3 (4-mil Cathode)
4=Device Type 4 (2-mil Cathode)



LOAD CURRENT (I_A)

1 = 2A 2 = 4A 3 = 6A
4 = 8A 5 = 10A 6 = 12A
t = 0.5 μs/DIV. T = 125°C
I = 2A/DIV.

Figure 3-18.
Turn-Off Characteristics for GTO-Thyristor with Varying Load Current. Input Source (V_{goc}, L_{gs} Kept Constant) [I_A, I_{gq}]=f(t), R_L Parameter Device Type 3 (4-mil Cathode)

current, $t_f \sim 200$ nanoseconds.

Figure 3-19 is a graph characterizing turn-off gain and storage time as a function of load current for the family of curves of Figure 3-18 and conditions given above.

10. Switching Performance

The data plotted in the graphs of Figures 3-20, 3-21, and 3-22 characterize the switching behavior for Device 2 (8 mil cathode), Device 3 (4 mil cathode) and Device 4 (2 mil cathode), respectively, over the temperature range from 25°C to 125°C.

Figures 3-20a, 3-21a, and 3-22a show the storage time t_s with V_{goc} as parameter. Device 2 could not be operated at $V_{goc} = -5V$, Device 3 functioned safely up to +65°C for $V_{goc} = -5V$. Device 4 operated safely over the full range for this low negative gate bias.

In Figures 3-20b, 3-21b, and 3-22b the rise time t_r and the fall time t_f are graphed. The current at the "tail break" is also given in ($\%I_T$). For instance, Device 3 had an initial tail current of $2\%I_T$, i.e., 160mA @ 65°C.

The rise time is identical for all devices, about 380 nanoseconds at 125°C. At lower temperatures, however, the rise time becomes longer for devices with narrower cathodes.

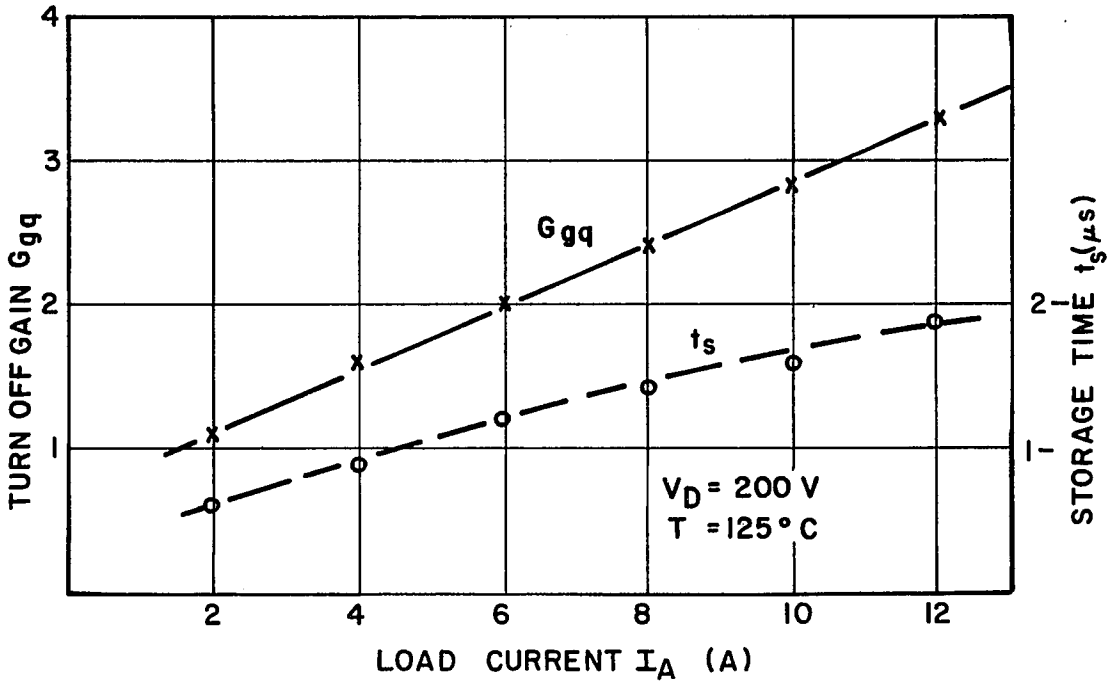


Figure 3-19.
Turn-Off Gain and Storage Time for GTO Thyristor with Varying Load Current Input Source (V_{goc}, L_{gs}) Kept Constant Device 3 (4-mil Cathode)

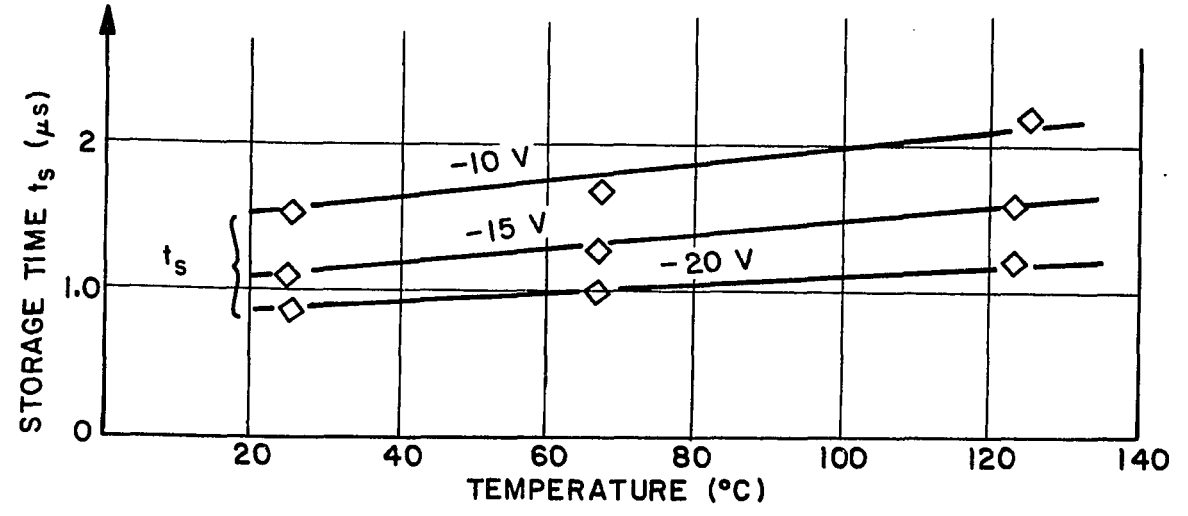


Figure 3-20a. Storage Time t_S=f(T)

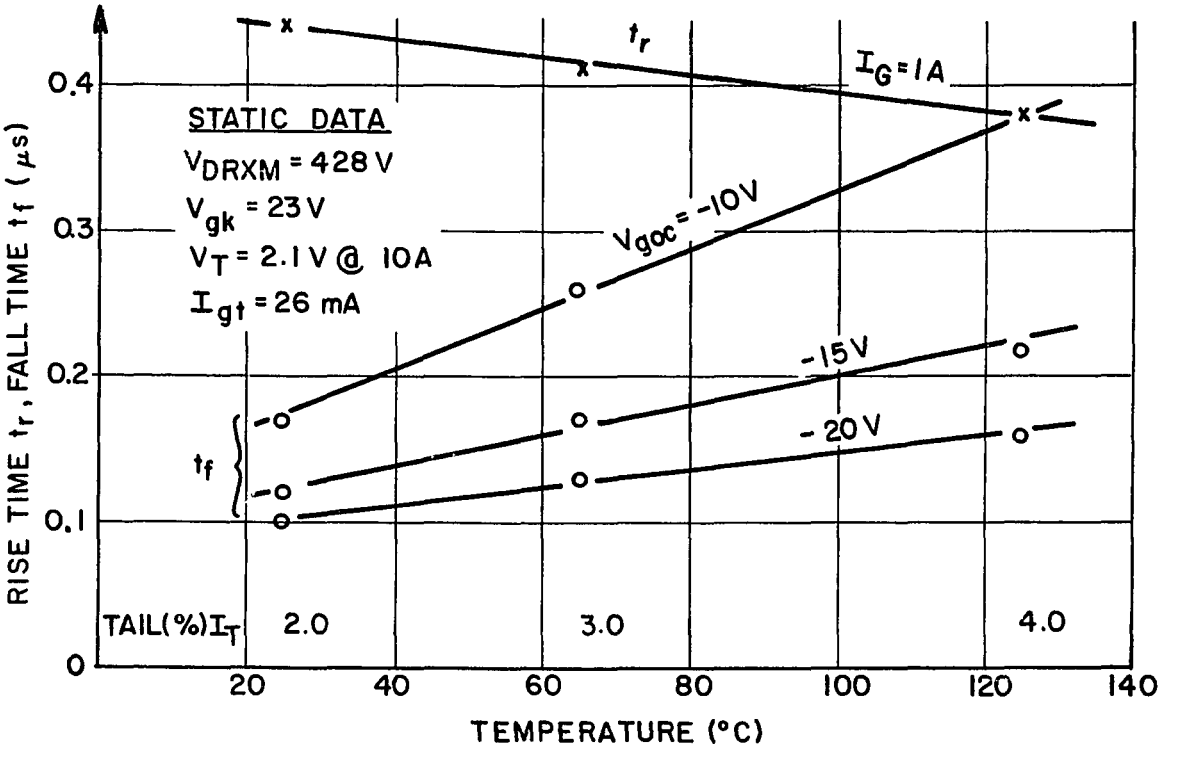


Figure 3-20b. Rise Time and Fall Time [t_r,t_f]=f(T)

Figure 3-20.
Switching Performance of GTO Thyristor as Function of Temperature. Device 2 (8-mil Cathode)
Conditions: I_T=8 A=constant, V_D=200 V, L_{gs}=4.6 μH

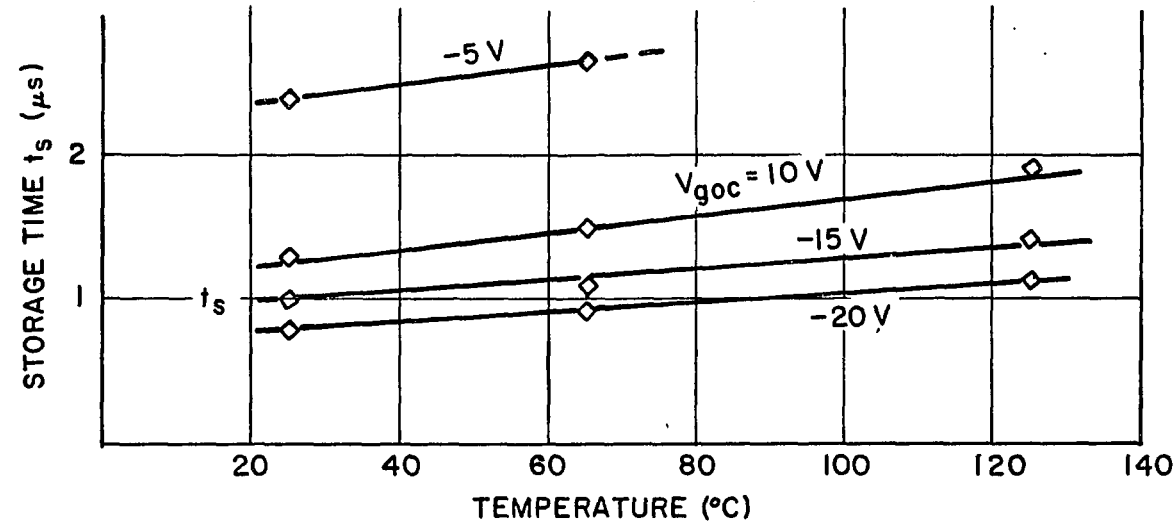


Figure 3-21a. Storage Time t_S=f(T)

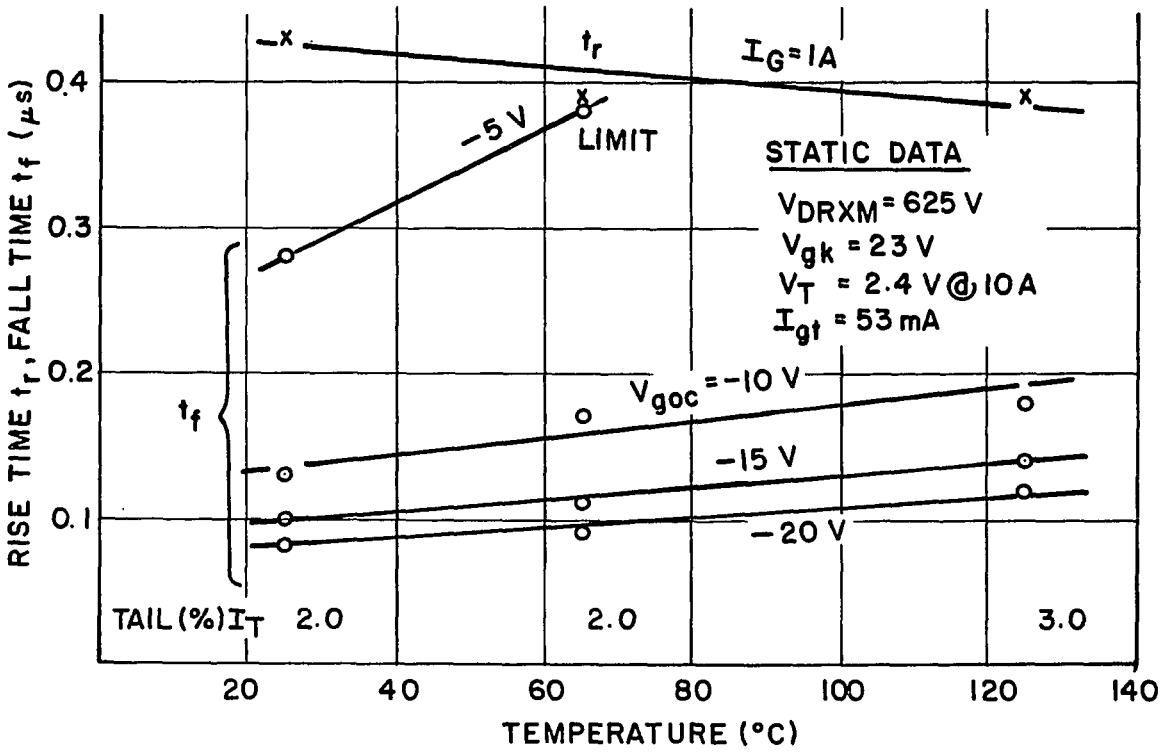


Figure 3-21b. Rise Time and Fall Time [t_r,t_f]=f(T)

Figure 3-21.
Switching Performance of GTO-Thyristor as Function of Temperature. Device 3 (4-mil Cathode)
Conditions: I_T=8 A=constant, V_D=200 V, L_{gs}=4.6 μH

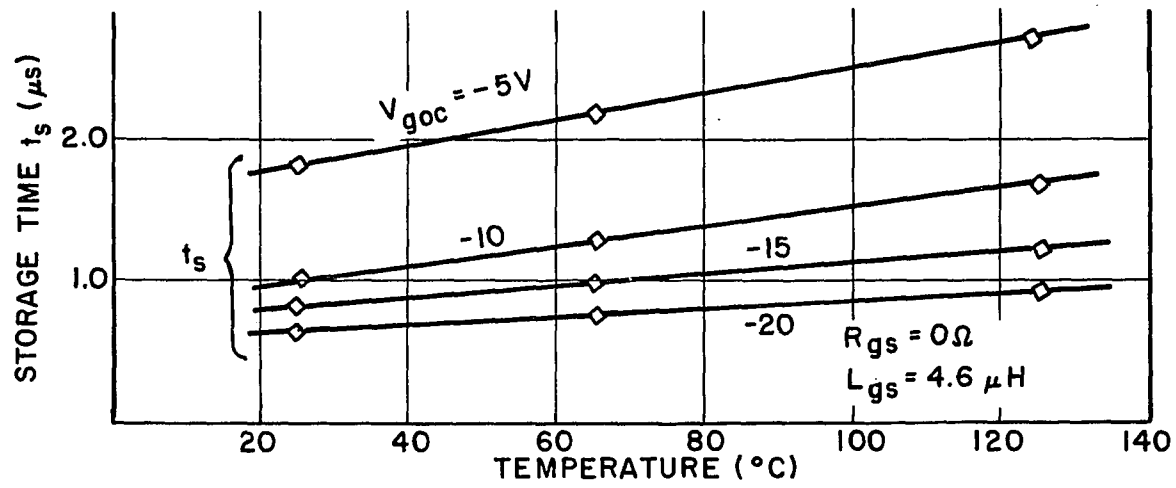


Figure 3-22a. Storage Time t_S=f(T)

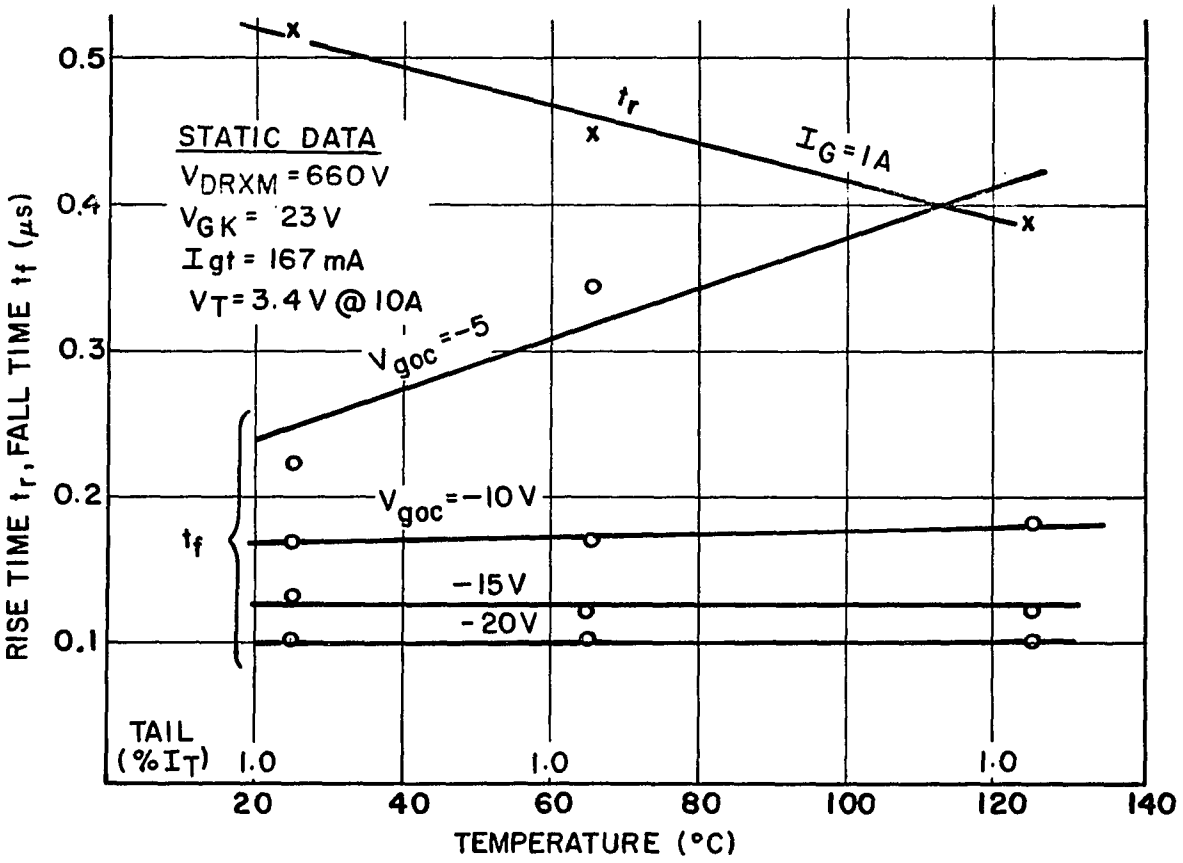


Figure 3-22b. Rise Time and Fall Time [t_r,t_f]=f(T)

Figure 3-22.
Switching Performance of GTO-Thyristor as Function of Temperature. Device 4 (2-mil Cathode)
Conditions: I_T=8 A=constant, V_D=200 V, L_{gs}=4.6 μH

The trend for the fall time is just in the opposite direction. The narrower the cathode width, the shorter t_f becomes. In Figure 3-22b we notice that for a gate source voltage larger than 10V the fall time becomes practically independent of temperature, the fall time t_f = 200 nanoseconds @ V_{goc} = 20V.

The peak gate current I_{gqm} required to obtain the switching times plotted in Figures 3-20 to 3-22 is given in Figure 3-23a for Device 2, in Figure 3-23b for Device 3, and in Figure 3-23c for Device 4, respectively. As can be seen lowest current $I_{gqm} \sim$ 1.5A is required for Device 4 (2 mil cathode) at V_{goc} = -5V, corresponding to a turn-off gain $G_{gq} \sim$ 5.3, for a storage time $t_s \sim$ 2.7μs (Figure 3-22a) and a fall time $t_f \sim$ 0.42μs (Figure 3-22b) @ T = 125°C.

Considering now the performance of Device 3 for example, it is noteworthy that simultaneously a fast rise time of ∿ 0.4μs was obtained and the gate trigger current of 50mA as well as the on-state voltage of 2.4V could be kept rather low. Usually, a device with such excellent turn-off characteristics would have a rise time of ∿ 1.5μs, a gate trigger current of ∿300mA, and an on-state voltage of ∿4V. The reason for the desirable combination of fast t_r and t_f, and low I_{gt} and V_T can be found if we investigate the spreading resistance profile of such devices more closely by probing the structure along several vertical passes [74-2, 79-4].

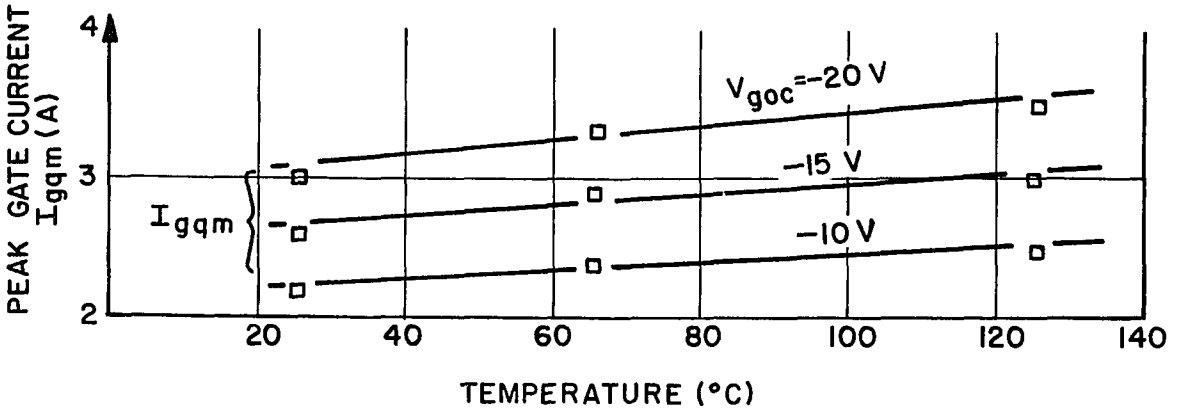


Figure 3-23a. I_{qm}=f(T), V_{goc} Parameter, 8-mil Cathode

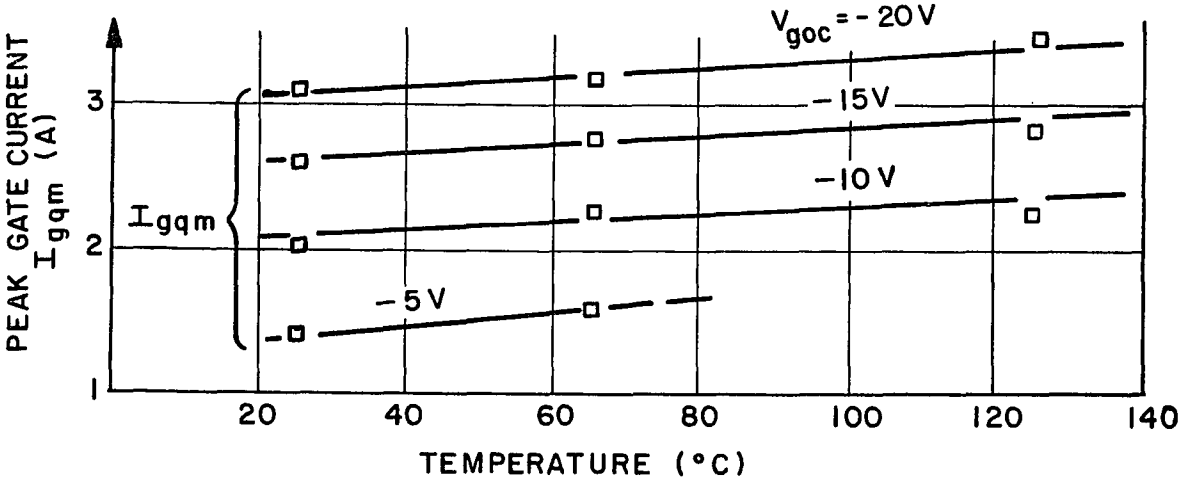


Figure 3-23b. I_{gqm}=f(T), V_{goc} Parameter, 4-mil Cathode

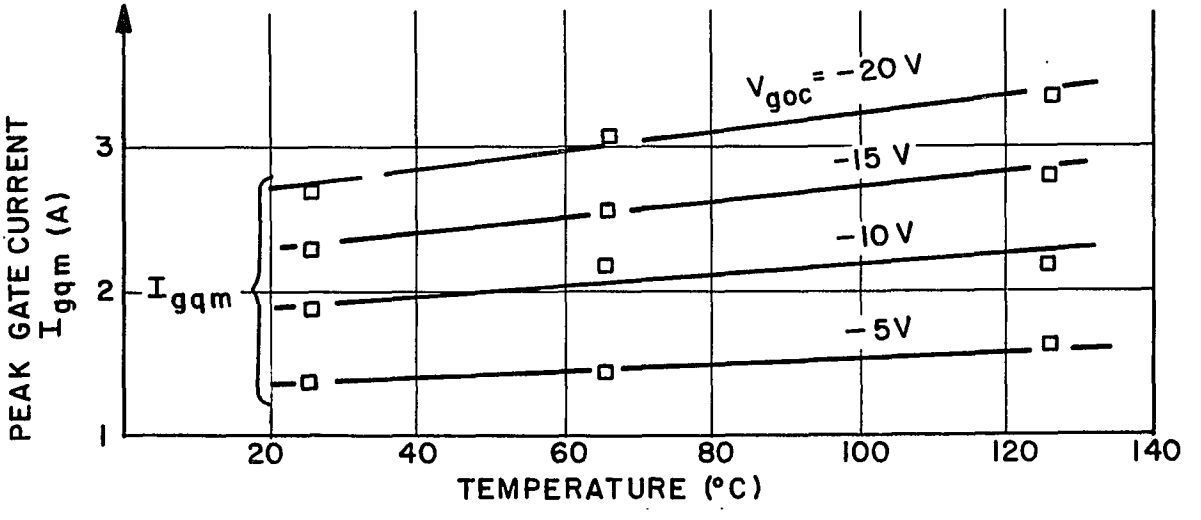


Figure 3-23c. I_{gqm}=f(T), V_{goc} Parameter, 2-mil Cathode

Figure 3-23.
Peak Gate Current Required for Turning Off a GTO Thyristor as Function of Temperature and Negative Gate Bias
Conditions: I_T=8 A=constant, V_D=200 V, L_{gs}=4.6 μH

11. Gold Distribution and Life Time

Figure 3-24 shows the vertical spreading resistance variation of the device taken through the p+-gate toward the anode along $\overline{CD}$ (see insert). The center junction is located about 36μ from the surface. The resistivity throughout the N^--region is >1000Ωcm. The entire N-base is upconverted from its initial value of approximately 30Ωcm. Thus, we assume that the Au-concentration is about 1.5×10^{14} corresponding to a life time $\tau_n \sim 0.5\mu s$ in the n-base[66-2]. The p-base in this region will have an even lower life time value.

Now we turn to Figure 3-25 in which the spreading resistance is taken through the N^+ cathode, again vertically toward the anode along pass $\overline{AB}$. The interesting fact here is that in the vicinity of the center junction, the starting resistivity is preserved (30Ωcm) and upconversion becomes noticeable only about 50μ into the n-base with a pronounced increase in direction of the anode. The difference in this spreading resistance profile from that of Figure 3-24 suggests that Au was gettered by the heavily doped phosphorus emitter above this region[72-1]. As a consequence the active gold distribution in the device is such that the life time is kept high (>1.0μs) in the p-base and in the n-base adjacent to the center junction while it is low (∿0.5μs) in the vicinity of the anode. The high life time keeps the npn gain reasonably high and accounts for the low I_{gt} and the fast t_r.

The low life time limits the anode emitter efficiency and also causes a rapid recombination of the stored charge in the n-base, the majority of which is located close to the anode junction[79-3]. Thus, the tail-effect is minimized.

Device	A_{cath} (mm^2)	L_x/L_n —	$J_{o(max)2d}$ (A/cm^2)	#Sites —	L_y/L_n —	$J_{o(max)3d}$ (A/cm^2)
D_1	.026	13.3	3440	4	25.4	87000
D_2	.029	5.73	1265	12	25.4	32000
D_3	.024	2.85	753	48	10.8	8000
D_4	.024	1.6	462	82	10.8	5000

Table 3-2. Peak Current Density for GTO during Turn-off.

$J_{o(max)2d} \equiv$ two-dimensional; uniform line turn-off

$J_{o(max)3d} \equiv$ three-dimensional; single spot/site turn-off

$\bar{J}_{cath} \sim 300\ A/cm^2$, $\bar{J}_{(on)} \sim 65\ A/cm^2$ for total chip. $L_n \sim 40\ \mu$

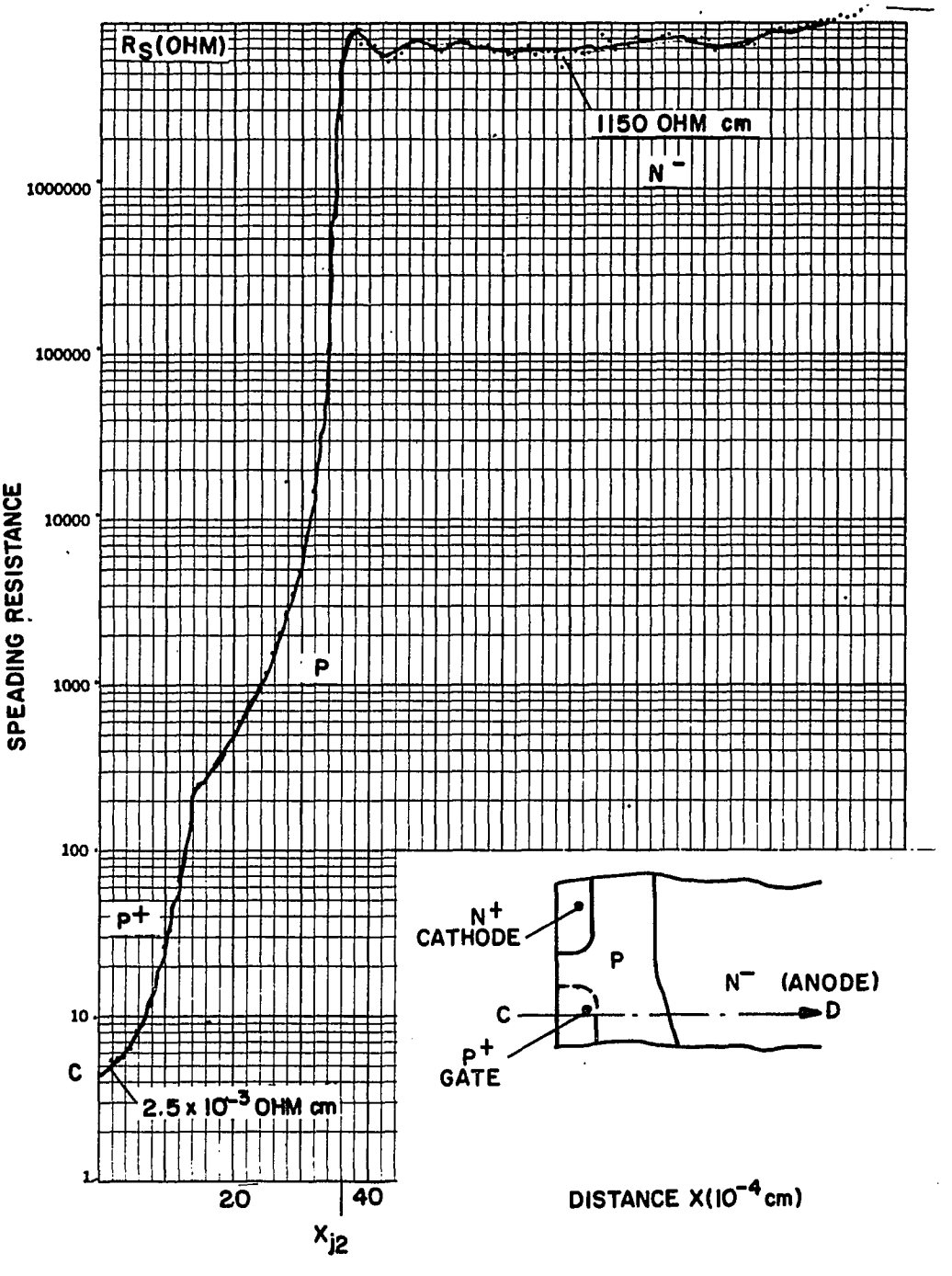


Figure 3-24.
Two-Point Probe Spreading Resistance Profile (C-D) through P^+ Gate showing Total Up Conversion of N^- Region. (Insert shows Schematic of Cross Section and Probe Travel Pass)

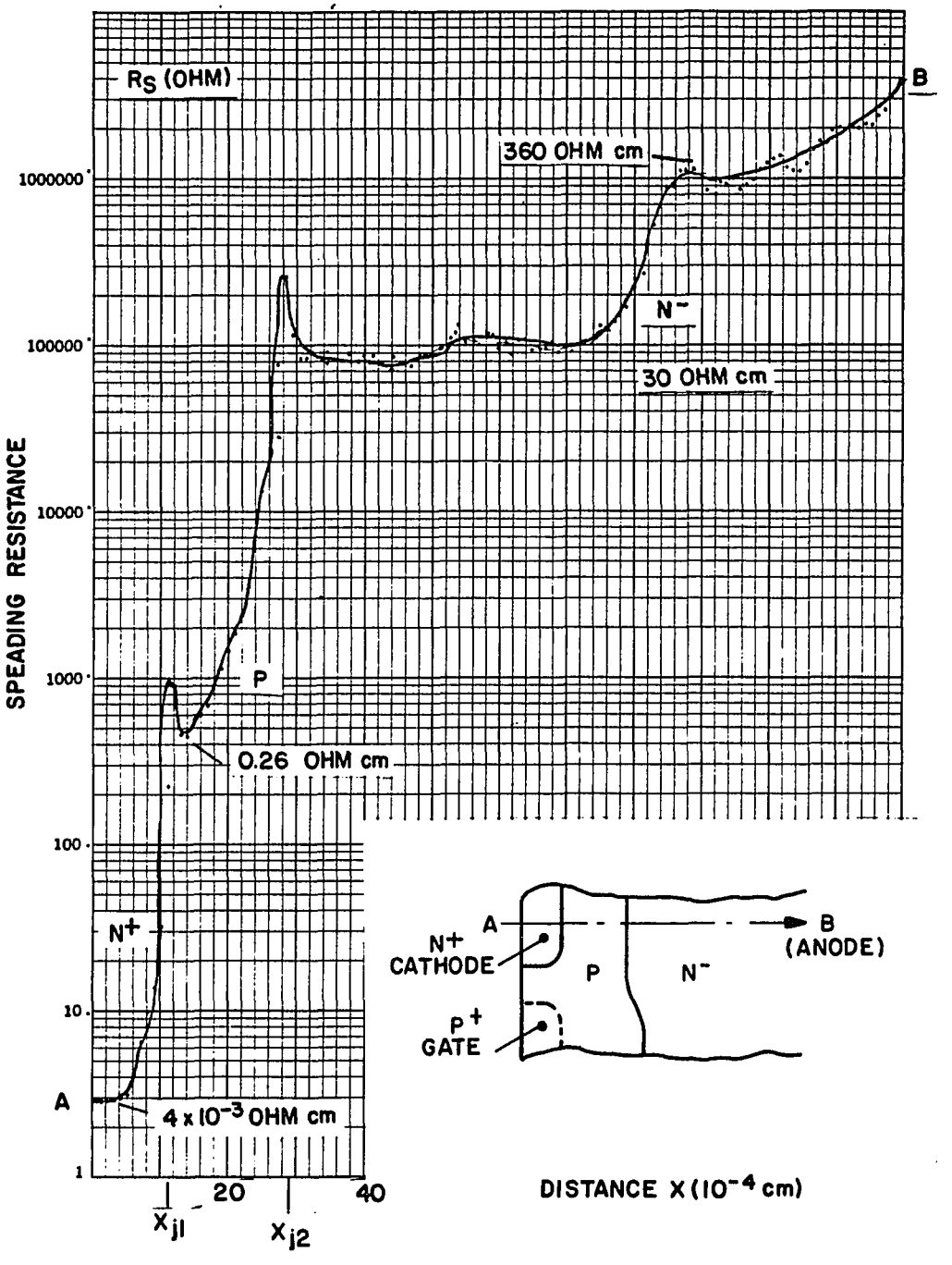


Figure 3-25.
Two-Point Probe Spreading Resistance Profile (A-B) through N^+ Cathode Showing Partial Up Conversion of N^- Region in Direction of P^+ Anode (Insert shows Schematic of Cross Section and Probe Travel Pass)

12. Power Switching Capabilities

With the results presented in the foregoing sections and discussions on safe operations it is now possible to evaluate the power switching capability of the high speed-high voltage Epi-base structure.

The total energy absorbed per cycle in a device is in general

$$E_{D\ tot} = \int_0^{t_r} I_A(t)V_A(t)dt + V_T I_T \left[(F_D T) - (t_r + t_{f1})\right]$$

$$+ \int_{t_s}^{t_{f1}} I_A(t)V_A(t)dt + \int_{t_{f1}}^{t_{f2}} I_A(t)V_A$$

$$+ \int_0^{t_{p(on)}} I_G(t)V_{GK}(t)dt + \int_{t_s}^{t_{p(off)}} I_{gq}(t)V_{gq}(t)dt \qquad 3\text{-}1$$

where F_D is the duty factor and T is time of one total period; $t_{p(on)}$ is the duration of the "On" pulse, and $t_{p(off)}$ is the duration of the "Off" pulse.

We choose as an example Device 3 @ T = 125°C and evaluate the integrals in Equation 3-1 with the aid of Figures 3-10b, 3-11, 3-16, and Figure 3-21. Operation is assumed for I_T = 8A and V_D = 400V, the pulse duration for turn-on and turn-off is set for $t_{p(on)} = t_{p(off)}$ = 3μs. The load is assumed to be R_L = 50Ω, resistive. The turn-on

gate current is $I_{G(on)} = 1.0A$ and $V_{G(on)} = 1.0V$. For turn-off $V_{goc} = -15V$ and a series inductance $L_{gs} = 4.6\mu H$ connects the gate.

The turn-on energy, assuming a quasi linear change of current and voltage in the output, is then

$$E_{t(on)} = E_{G(tr)} + E_{A(tr)} \tag{3-2}$$

$$E_{G(tr)} = V_{G(on)}\ I_{G(on)}\ t_{p(on)} \tag{3-3}$$

$$E_{A(tr)} = \frac{1}{4}\ V_D I_T t_r \tag{3-4}$$

The turn-off energy is

$$E_{t(off)} = E_{G(t_{f1})} + E_{G(t_{f2})} + E_{A(t_{f1})} + E_{A(t_{f2})} \tag{3-5}$$

$$E_{g(t_{f1})} + E_{G(t_{f2})} = \frac{1}{2}\ V_{goc} I_{gqm} t_s + \frac{1}{2}\ L_{gs} I_{gqm}^2 \tag{3-6}$$

$$E_{A(t_{f1})} = \frac{1}{4}\ V_D I_T t_{f1} \tag{3-7}$$

$$E_{A(t_{f2})} = V_D\ kI_T \tau_{pA} \tag{3-8}$$

where k is the ratio of "tail break current" to on state current and τ_{pA} is the hole life time in the vicinity of the anode.

The resultant components of absorbed energy/cycle are given in Table 3-3.

$E_{G(tr)}$	$E_{A(tr)}$	$E_{G(t_{f1})}$	$E_{G(t_{f2})}$	$E_{A(t_{f1})}$	$E_{A(t_{f2})}$	E^{*}_{on}
3	320	27	21	160	96	166

Table 3-3 Components of Dissipated Energy/Cycle in μJoules for GTO (Device Type 3).
I_A = 8A, V_D = 400V, T_j = 125°C, Res. Load,
*) f = 50kHZ, 50% Duty Cycle

Summing up all components, the total energy per cycle is then E_{tot} = 793 μJoule. It follows that for 50kHZ the power dissipation is approximately 40 watts. The thermal resistance for this device mounted in a TO-3 case is at worst Θ = 1.2°C/Watt. Therefore, the maximum allowable case temperature is 78°C.

Above assumptions and calculations show that this device is capable of switching a load of 1560 Watts at a frequency of f = 50kHZ.

Turning back to the discussion about power switching capability with respect to cost (pp. 44), we are now able to fit this device in the graph of Figure 3-2. The result is shown in Figure 3-26. There, a vertical "cost line" is added at the 50 kHz point on the abscissa and we see that in order to reach the projected boundary (broken line) of the GTO-Thyristor region, the cost per device would have to be 25¢.

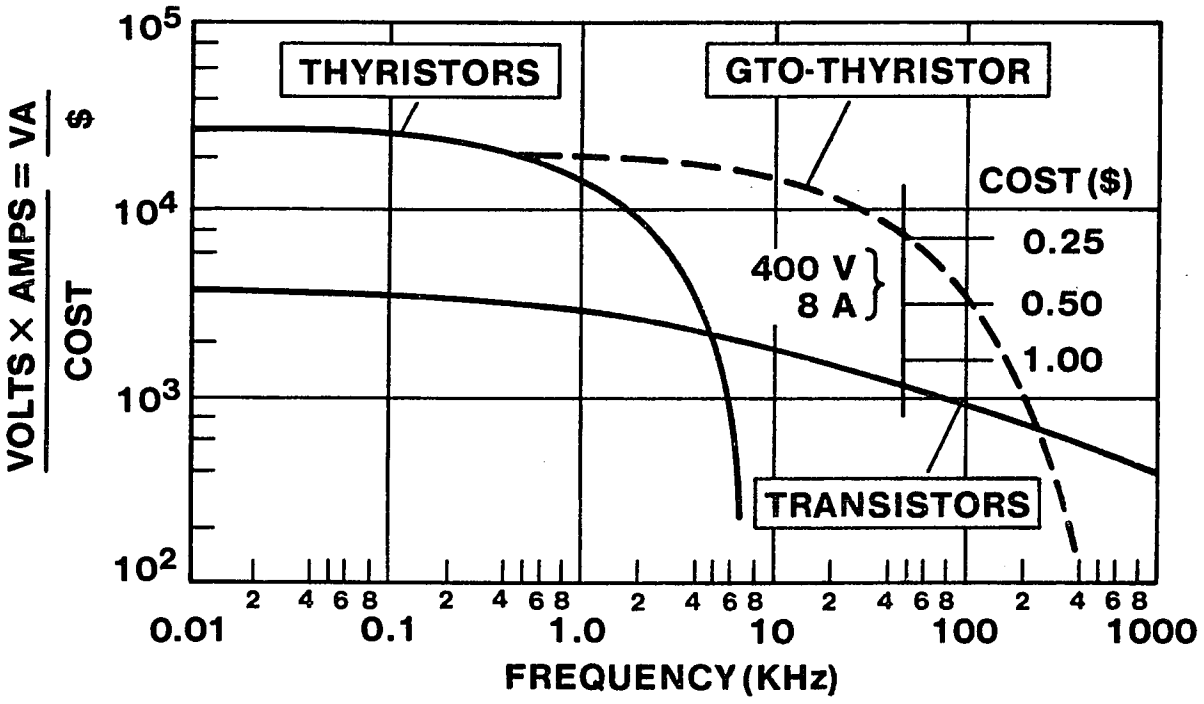


Figure 3 – 26. Comparison of Power-Switching Capability with Respect to Cost as a Function of Frequency for Thyristors, GTO's, and transistors (The cost Line at f = 50 kHz indicates where the GTO Type D3 would be in this graph for 400 V, 8 A operation using the data of Table 3 – 3)

The $1.00 cost intersection is certainly realistic if one is reminded that this graph was generated from a survey taken several years ago (see Footnote, pp. 44).

From the switching times obtained it is certainly possible to operate this device at 100kHz. Therefore, if the case temperature can be held at a maximum temperature of 38°C ($P_D \sim 74W$) the cost line can be moved up to 100 kHz. It is apparent that for these considerations the GTO is quite compatible with transistors as an economical power switch.

IV. SERIES SCHOTTKY BARRIERS AND DYNAMIC BALLASTING

In this chapter principles for improvements of the state-of-the-art in GTO devices are described in a brief and general manner. Experimental proof is given for new concepts which were introduced by the author. These concepts deal with anode shorts and series Schottky Barriers, and measures to defocus current filaments (Dynamic Ballasting).

A. Anode Shorts and Schottky Barriers

An effective method of improving turn-off characteristics of GTO's is to introduce anode shorts[75-1, 78-1]. If these shorts are dimensioned properly and are placed most remote from the gate contact, the excess minority carrier charge in the n-base will be partially removed through those shorting resistances during turn-off. Also, the squeezed plasma will tend to be extinguished in this non-regenerative center section (see Figure 1-3, pp. 10). The anode shorts may be thought of as being by-pass transistors in parallel with the thyristor. Therefore, while turn-off is aided, turn-on is impaired.

1. Device Structure and Geometry

The cross section of a device having an anode short placed opposite the center of the cathode emitter is schematically shown in Figure 4-1. The general effect of an anode short on turn-off was described above. In particular, turn-off gain is increased; fall time, tail current magnitude and tail decay time are decreased. Turn-off characteristics show an improvement similar to that achieved by gold diffusion. Since the lifetime can remain high, a lower on-state voltage drop is obtained[78-1]. Further, control problems associated with gold diffusions are

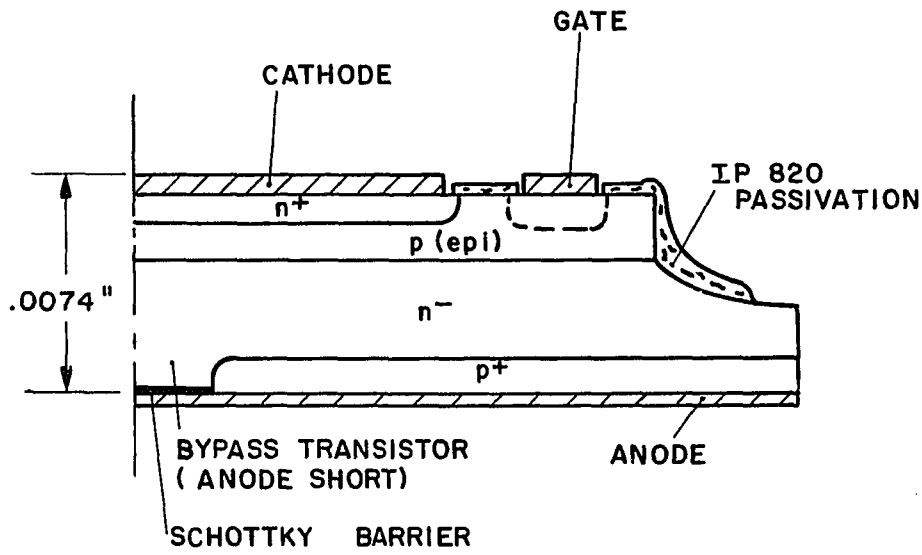


Figure 4-1.
GTO Structure showing Anode Short (By-Pass Transistor) and Series Schottky Barrier aligned with Center of Cathode

eliminated.

The drawback for anode shorts becomes clear if we examine such a structure with respect to turn-on and the degree of interdigitation (cathode subdivision, to reduce the lateral turn-off distance L_x).

Assume in Figure 4-1 the N^- region in the emitter center is ohmically connected to the anode metalization. Then, upon applying a positive bias to the gate-cathode junction, the NPN section is turned on. Initially, current is flowing through the short, setting up a lateral component.

The resulting lateral voltage drop constitutes the negative forward bias of the P^+N^- anode junction. Injection is strongest in the anode region opposit the cathode edge. The diode knee voltage, i.e., $\sim$0.7 volt for silicon, has to be reached before significant hole injection will occur, and only then can the device be triggered into the conduction state. Therefore, narrow cathode stripes and conductivity modulation of the N^- region may prevent turn-on altogether. This effect shows a strong temperature dependence, because the current gains α_1 and α_2 drop with decreasing temperatures.

The problem is eliminated if the ohmic contact is replaced by a Schottky barrier[79-1], as shown in Figure 4-1. In case, the barrier height is equal to that of the silicon PN junction and the diode characteristics in the forward direction are similar, lateral bias is not required. Device turn-on proceeds as for a standard thyristor.

Minority carrier injection in the Schottky barrier region is practically absent, however, and consequently the features aiding turn-off of this non-regenerative section are preserved.

Experiments were carried out to prove the series Schottky barrier concept. Devices with a geometry as shown in Figure 4-2 were chosen as test vehicles. The cathode geometry is the same as that of Device 2 in Figure 3-6 (bottom row, center), except that for this modified version the cathode fingers are portions of a continuous area, and the tips are rounded off. The gate envelopes this entire cathode pattern.

In assembly, a double gate contact clip is soldered to the regions just outside of the small center fingers. The cathode clip is attached in the middle of the cathode bus.

The rectangular center region (appr. 22 mils wide) at the back of the chip does not contain a P^+ anode diffusion. It is rendered inactive as a thyristor.

When this device is in the "on" state and a negative gate bias is applied, the electron-hole plasma is pinched toward the center of the individual cathode stripes. Because of the taper, the plasma is driven from the tips into the non-regenerative center region. There it is extinguished. Thus, the center is equivalent to a transistor bypass.

Surface preparation and choice of metalization can be chosen such

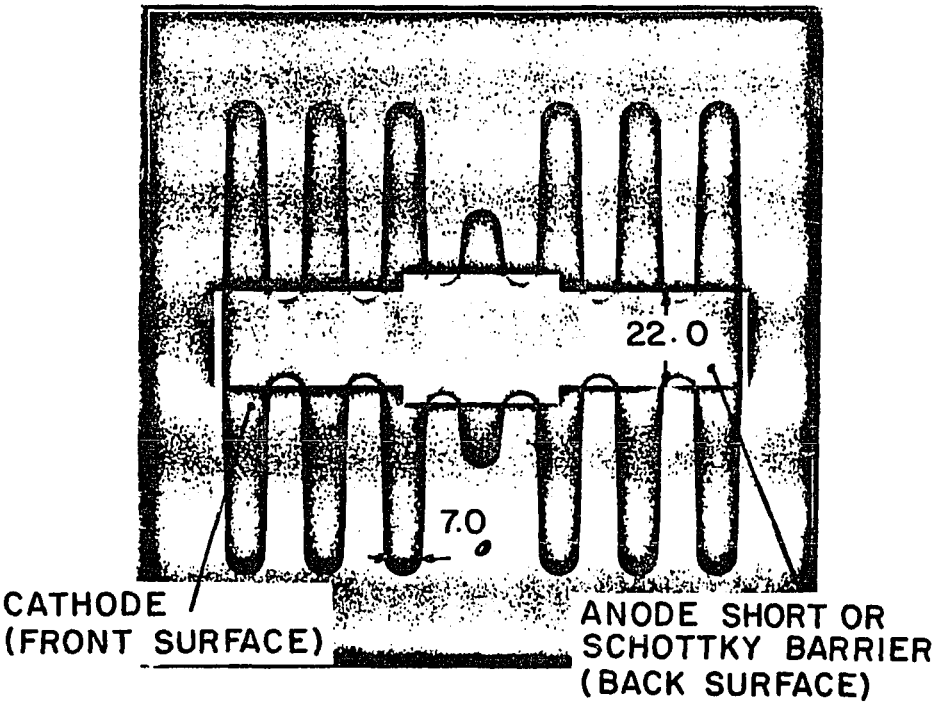


Figure 4-2.
Geometry Overlay of Cathode and Anode Surface showing non-regenerative Center Region (Anode Short or Schottky Diode)

that either an ohmic contact is formed with the N-region on the back surface to produce an anode short, or that a Schottky barrier is obtained. The metalization will always form an ohmic contact with the P^+ anode, however.

For the experiment described here nickel, applied using a special electroless plating process, was used. When sintered at 580°C for 30 min. on a lapped (rough) surface an ohmic contact was obtained, whereas on a chemically polished (smooth) surface the nickelsilicide formed a suitable Schottky barrier. An alternate choice for forming a Schottky barrier is platinumsilicide.

2. Turn-On With and Without Schottky Barrier

The effect of a short versus a Schottky diode on the VI-characteristics for otherwise identical devices is illustrated in Figure 4-3. Junction depth and impurity profiles were very similar to devices, whose spreading resistance is given in Figure 3-8. However, the epi-base resistivity was lowered from $\sim$0.28Ω cm to 0.11Ω cm, and the gold diffusion was omitted.

On the left hand side in Figure 4-3, the IV-characteristics of the device with an anode short are displayed (G400-1). The family of traces on top shows the device before turn-on. We see essentially an NPN transistor with β_1 varying from 0.4 to 0.7 up to 1.06mA. The saturation voltage rises about linearly up to 0.7 volts for a base drive I_g = 2mA. Thus, we conclude that up to this point the device

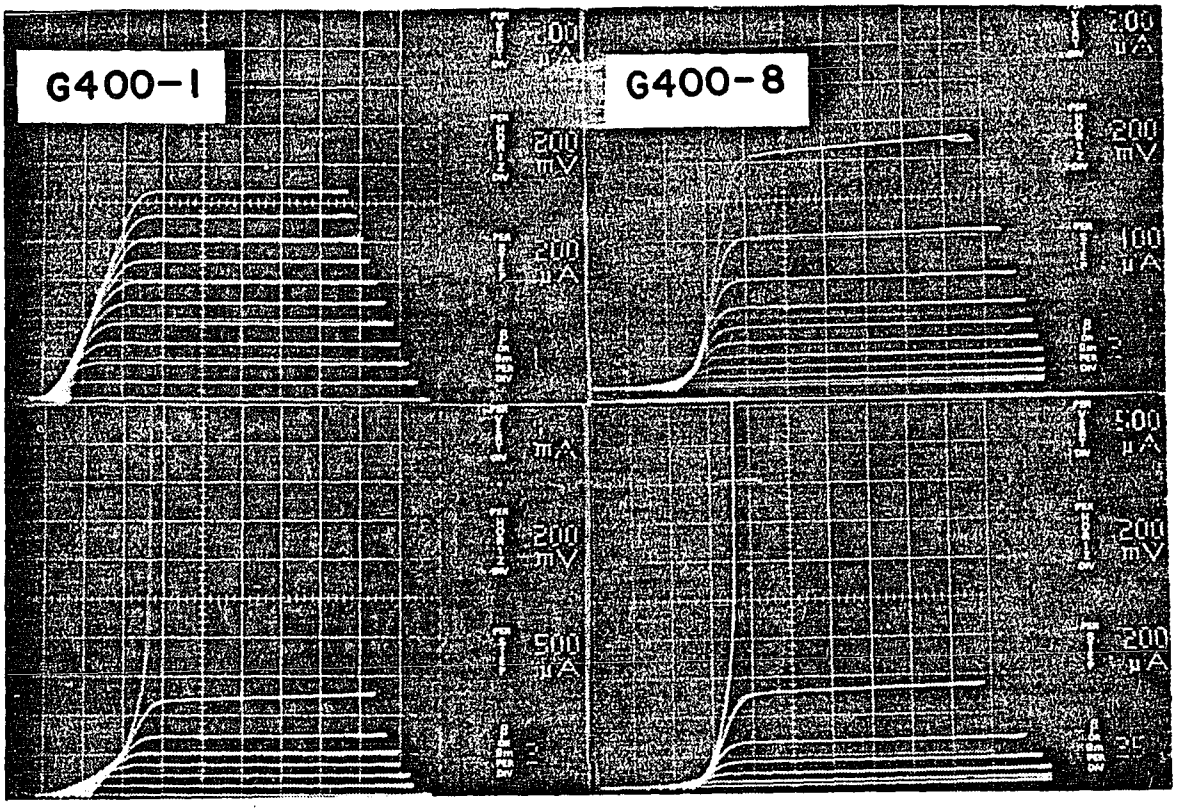


Figure 4-3.
VI Characteristics of GTO showing Difference in Turn-on for Device with Anode Short (G400-1, Left) and Device with Series Schottky Barrier (G400-8, Right)

is dominated by by-pass current through the anode short.

As the base drive is increased, and the saturation voltage reaches the "diode knee" of the P^+N anode emitter, a sudden gain increase and triggering into the on-state is accomplished. We conclude that now the device is dominated by "thyristor action". When the sum of the current gains ($\alpha_1 + \alpha_2$) reaches unity the device turns on ($I_{gt} \sim 3.5mA$ @ $V_D \sim 2V$).

On the right hand side of Figure 4-3 the IV-characteristics of the device with a series Schottky barrier are displayed (G400-1). Again, the top family of curves show the device before turn-on. Here we see a distinct offset, as normally observed for a double injection device. Also, the gain is increasing rapidly. Both transistor sections are active as soon as base drive is applied, and the Schottky barrier by-pass current is only a fraction of that observed for the case with the anode short. The device is dominated by thyristor action throughout the entire range of operation. Turn-on occurs now for $I_{gt} \sim 1.2mA$ @ $V_D \sim 2V$, as can be seen from the IV-traces displayed in the lower right hand side of Figure 4-3.[1]

---

[1] Of interest for the determination of α_1 and α_2 in thyristors are the measurement technique and algorithm developed by R. Amantea[79-5].

3. Turn-On Sensitivity and Turn-Off Capability

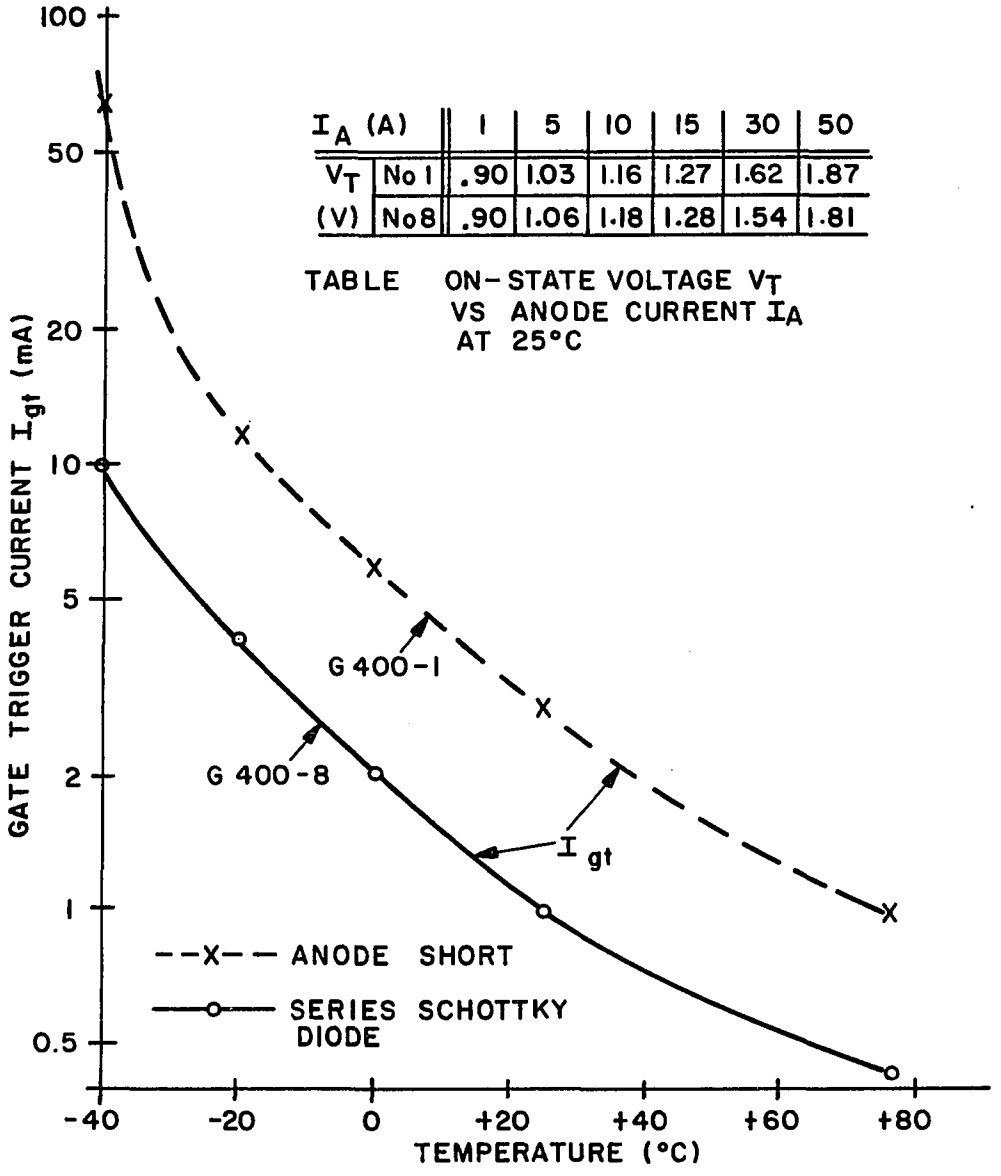
In Figure 4-4 we have plotted the turn-on sensitivity as a function of temperature for the two devices discussed in the previous section. The gate trigger current was measured with an anode supply voltage V_D = 12V and a load resistance of R_L = 3Ω.

The inserted table shows the forward voltage drop V_T over a current range from 1.0A to 50A. As may be noticed in that respect, there is no discernible difference between the device with the anode short and the series Schottky diode.

In contrast, the gate trigger currents show a pronounced difference. The Schottky barrier device is considerably more sensitive. Especially at low temperatures (-40°C) the shorted anode device (G400-1) requires $I_{gt} \sim$ 70mA, while for the device with the series Schottky barrier (G400-8) $I_{gt} \sim$ 10mA only.

The turn-off capability of both devices is given in Figure 4-5. In this test the GTO's were operated in cathode load configuration, the load being grounded, and the anode being directly connected to the supply voltage V_D = 12V. To achieve turn-off a transistor connected to the gate was turned on, pulling the gate close to the ground potential ($\sim$ + 0.2V)[1]. The peak gate gate current I_{gqm} was

[1] A special turn-off circuit employing a small thyristor in parallel with a transistor was developed[78-2] showing advantages for turn-off. The data given in Figure 4-5 were obtained using just a single transistor, however.



I_A (A)		1	5	10	15	30	50
V_T (V)	No 1	.90	1.03	1.16	1.27	1.62	1.87
	No 8	.90	1.06	1.18	1.28	1.54	1.81

TABLE ON-STATE VOLTAGE V_T VS ANODE CURRENT I_A AT 25°C

Figure 4-4.
Turn-on Sensitivity as Function of Temperature for GTO with Anode Short (dashed line) and Series Schottky Diode (solid line)

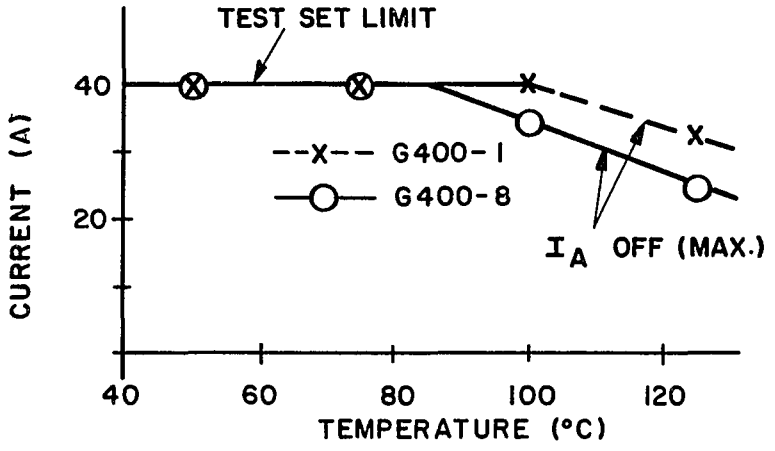


Figure 4-5.
Maximum Turn-off Capability for GTO as Function of Temperature

approximately 5A.

As shown in the graph (Figure 4-5) for temperatures below +90°C both device types could turn-off 40A, the test set limit. At 125°C the Schottky barrier sample had only lost 25% of its turn-off capability over the sample with the shorted anode ($I_{T\ off\ (max)}$ = 24A compared to 32A, respectively).

This result demonstrates in a straightforward and explicit manner the effectiveness of the series Schottky barrier. The turn-on sensitivity in GTO's is restored, while the turn-off improvement gained from anode shorts is retained. Using this concept has made is possible to use non-regenerative regions in very narrow cathode geometries[79-1].

B. Dynamic Ballasting (Defocusing)

In the work on high speed device optimization and in experiments with anode shorts there were still failures observed (burn-out spots) which were evidently caused by high current density filaments. A pipe (about 40 to 50 micron in diameter) was molten through the silicon from the front to the back of the chip. The location of these pipes was not random in the cathode, but rather distinctly in an area most remote from the gate contact.

A typical example is shown in Figure 4-6. The entire chip is shown on top (Figure 4-6a). A small hole is visible in the center cathode finger opposite the gate pad. The gate of this device was contacted with a single clip only. The burn-out spot is clearly visible in the

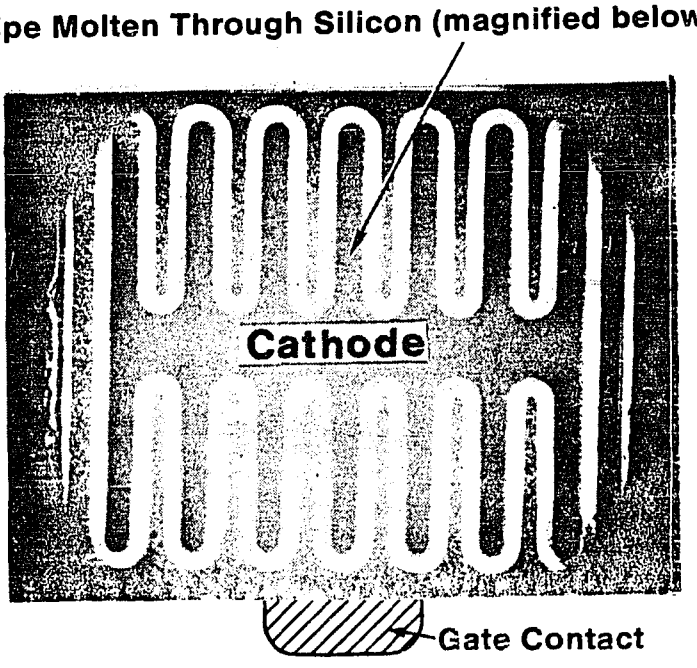


Figure 4 – 6a. Device Chip after Failure (Metal removed).

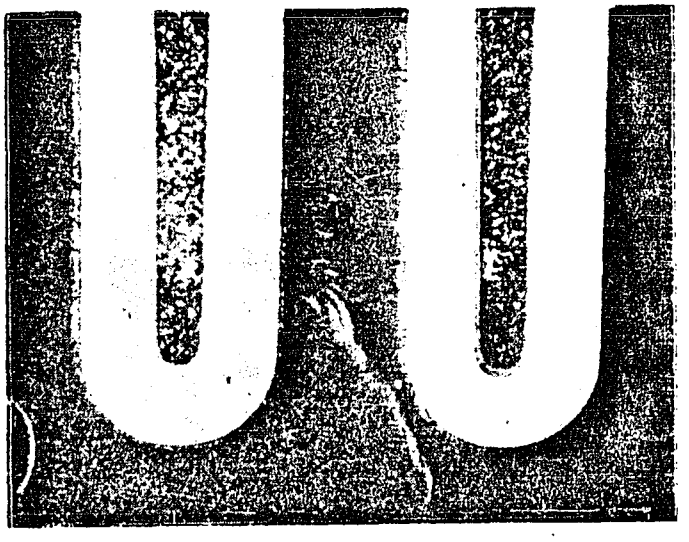


Figure 4 – 6b. Magnified View of Damaged Area

Figure 4 – 6. Turn-off Failure for GTO-SCR at Location most remote from Gate Contact.

magnified microphotograph below (Figure 4-6b).

In order to minimize such burn-out failures a method was thought that would prevent the formation of high current density filaments during the turn-off process. Dynamic Ballasting[77-1, 80-1] or defocusing was investigated and proved to be a very effective remedy.

1. Defocusing Principle and Device Structure

Figure 4-7 is the schematic cross-section of an epitaxial GTO structure in which the standard high concentration, phosphorus doped cathode is replaced with a lower concentration, resistive ion-implanted N layer. Also, the center of the cathode is insulated, only the edge is contacted with the metal electrode.

The resistive layer is dimensioned such that for turn-on and the on-state, while modest current densities exist in the device, we can expect normal thyristor behavior; i.e., fast turn-on with high sensitivity and low forward voltage drop.

In the process of turn-off, however, when the electron-hole plasma is being squeezed toward the center high current densities will tend to develop locally beneath the insulated cathode section. Then, the lateral current flow in the resistive region will cause a voltage drop along the PN junction, and the cathode becomes debiased in the direction of the center. Consequently, the current injection will decrease rapidly because of its exponential dependence on the junction bias voltage according to the diode law.

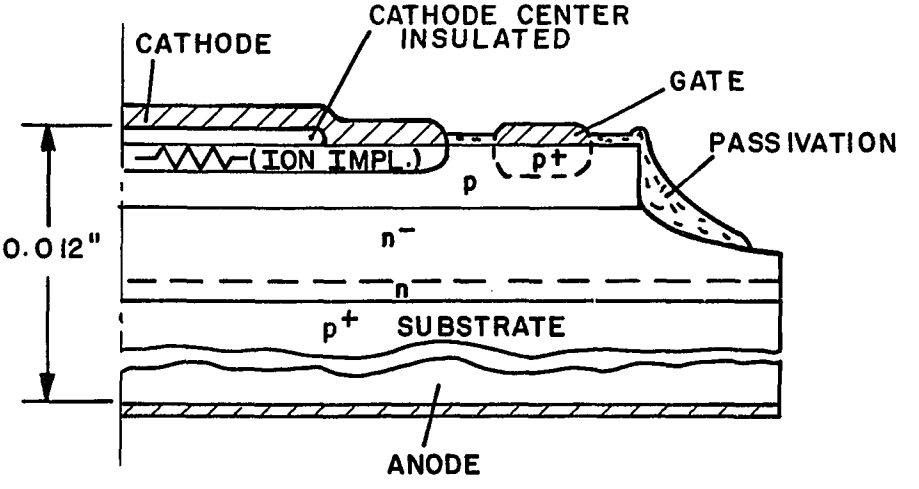


Figure 4-7.
Schematic of Epi-GTO featuring Resistive Cathode with Isolated Center to achieve Dynamic Ballasting (Defocusing)

Devices designed and fabricated for the experiments to investigate the effectiveness of the Dynamic Ballasting concept were of the geometry Type 3 (see Figure 2-8, bottom counter). The epitaxial p-gate layer was about 30 micrometer thick and had a resistivity of ∿0.12Ωcm. The epitaxial N^- region of the wide PNP base was about 50 micrometer thick with a resistivity of 50Ωcm, followed by a 20 micrometer wide, 2.0Ωcm layer to prevent early punchthrough. The 0.01Ωcm boron doped substrate served as the anode[1].

2. Turn-Off With and Without Dynamic Ballasting

The cathode load response $I_k = f(t)$ and the anode current $I_A = f(t)$ for devices with dimensions and physical parameters given in the previous section are shown in Figure 4-8. The turn-off circuit and conditions used were the same as those applied in the series Schottky barrier experiments.

The top traces are the turn-off characteristics for a device having a standard, heavily doped cathode of R_{sk} ∿0.7Ω/square. The turn-off gate pulse is initiated at t = 35 microseconds. We detect an initial current drop across the load (left), a storage time t_s = 15 microseconds, and a fall time t_f ∿4 microseconds, followed by a 25 microsecond tail period starting at a current of 1A.

The anode current (right) increases sharply when the gate turn-off pulse is applied, because the gate is grounded through the input driver and an additional low impedance path is provided.

---

[1]For "defocused" devices, Series 97H the Mask M04 (Figure B-1e) was substituted with Mask M05 (Figure B-1g, pp. 152).

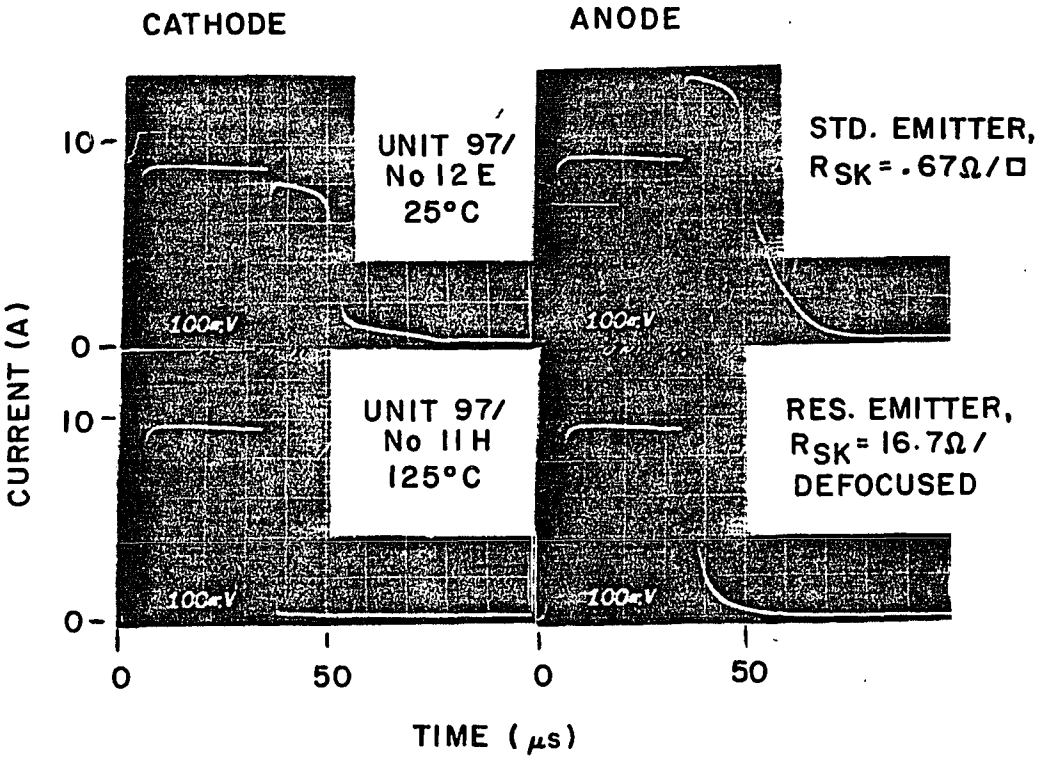


Figure 4-8.
Cathode Load Response I_K=f(t) (Left), and Anode Current I_A=f(t) (Right) for Epitaxial (N)PN⁻ N(P^+) GTO-Thyristor with Std. Diffused Cathode Emitter (Top) and Resistive, Defocused Cathode Emitter (Bottom) T=125° C, Vert.=2 A/Div, Hor.=10 μs/Div

During the tail period the anode current has still a considerable magnitude, starting with a value of 5A. The difference between anode current and cathode current is of course the gate current I_{gq}.

We see this device has a poor turn-off performance even at 25°C.

The bottom traces of Figure 4-8 are the turn-off characteristics for a device having an ion implanted cathode of ∿20Ω/square, metalized at the edge according to the schematic of Figure 2-7. Otherwise, structure and fabrication process were identical to the device above. Circuit conditions for turn-off remained also unchanged. The case temperature[1] was here raised to 125°C, however.

We see that in comparison to the non-ballasted device the storage time and fall time have drastically decreased, and the tail current through the load has just about vanished (left). The anode current (right) as well as the gate current pulse, and therefore also the turn-off energy are considerably diminished.

We observe this device has an excellent turn-off capability even at 125°C, which is the generally accepted upper temperature limit for reliable thyristor operation.

Figure 4-9 shows the turn-off portion for resistive cathode

---

[1] In these tests the GTO's were operated at low duty cycles. Therefore, the case temperature is close to the actual center junction temperature.

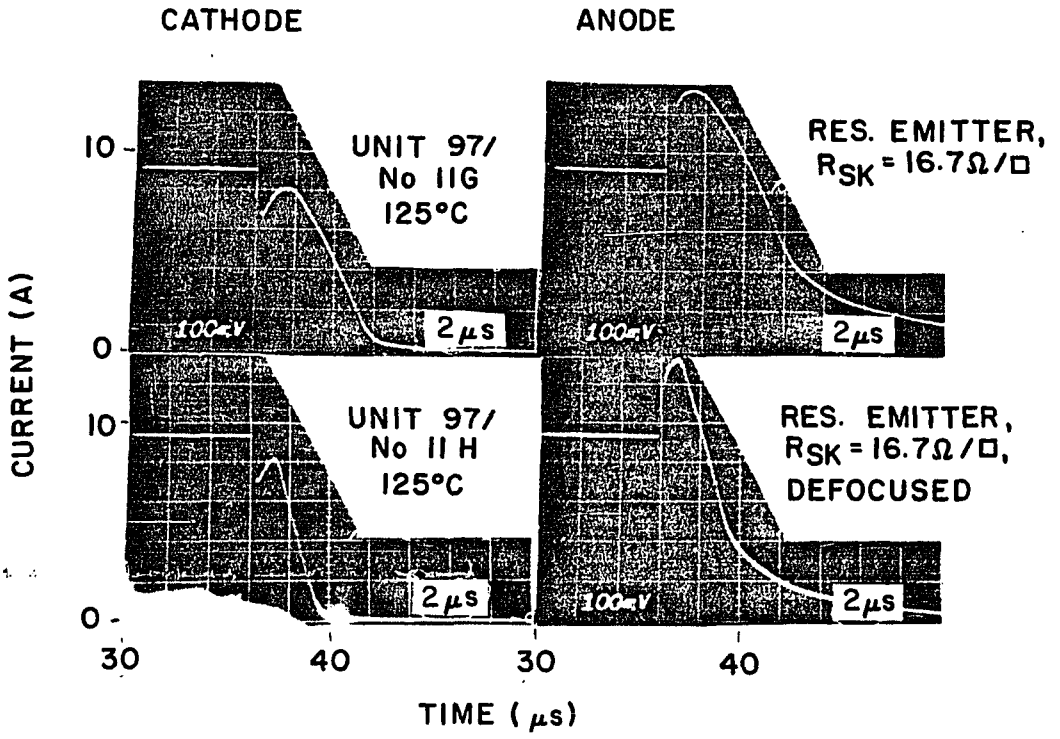


Figure 4 – 9. Turn-off Response for Epitaxial (N)PN⁻N(P^+) GTO in Cathode Load Circuit, I_k=f(t) (Left), I_A=f(t) (Right). Top Traces are for fully Metallized, Resistive Cathode; Bottom Traces are for Edge Metallized, Defocused Cathode. T=125°C, Vert.=2 A/Div, Hor.=2 μs/Div.

emitters on a 5X expanded time scale over the traces in Figure 4-8. The bottom traces are just an expansion of the ones of unit 97/11H in Figure 4-8. The total turn-off time ($t_s + t_f$) is only about 4 microsecond, the tail is indeed negligible, and the switching dissipation is small compared to the case for the standard cathode device (Figure 4-8 top).

The top traces in Figure 4-9 show a device (97/11G) with the identical resistive cathode as the one on the bottom. But here the entire cathode area is metalized. The response is slower and the switching dissipation is higher than for the "insulated cathode center" type. Yet, even in this case the ballasting appears to be rather effective over the standard cathode unit.

The shortened turn-off time, the reduction of the tail current, and increased turn-off capability at elevated temperatures are an indirect indication that for nominal values dynamically ballasted devices can be much safer operated than conventional GTO's

3. Summary of Results

The results of the experiments demonstrating the effect of dynamic ballasting are summarized in Table 4-1. Gate trigger current I_{gt}, forward voltage drop V_T, and maximum current turn-off capability are tabulated. The data represent averages of about 25 devices for

Geometry	I_{gt} (mA)		V_T (V)	Max. $I_{turn-off}$ (A)	
Std. G400 R_{sk}~.7 Ω/□	12.0	1.8	1.15	25	12
D3, PN-N^+ Epi R_{sk}~.7 Ω/□	.7	.06	1.22	9	2
D3, PN-N^+ Epi R_{sk}~20 Ω/□	.75	.10	1.48	15	13
D3, PN-N^+ Epi R_{sk}~20 Ω/□ + Defocusing	1.3	.22	1.53	18	14
	-40° C	+25° C	+25° C	+25° C	+125° C
D3, PN-N^+ Epi R_{sk}~7 Ω/□ + Defocusing	.3	0.06	1.28	9.3	8.5
	-60° C	+25° C	+25° C	+25° C	+150° C

Table 4-1. Effect of Resistive Cathode and Dynamic Ballasting (Defocusing) on GTO Temperature Behavior.

each test cell[1], except for the standard G400.

The desired characteristics are of course a small I_{gt} at low temperatures, a high $I_{T\ off\ (max)}$ at high temperatures and a low forward voltage drop V_T.

The first data line shows best results obtained for a conventional, anode shorted device with the geometry shown in Figure 4-2 (G400) and having a standard triple diffused doping profile. Such a device needs 12mA for turn-on @ -40°C, has a forward voltage drop of 1.15 volts @ 10A and 25°C, and it can turn-off 12A @ +125°C.

Compared with these results are the all-epitaxial test devices described in section IV B1. In particular, the second data line gives results for devices with a standard 0.7Ωcm cathode (Figure 4-8, top). As can be seen, this device is very sensitive (I_{gt} ∿0.7mA @ -40°C) for turn-on, however, it has lost its good turn-off capability at high temperatures (Now $I_{T\ off\ (max)}$ ∿2A).

The data shown in the fourth line are for the devices with an ion implanted cathode emitter of 20Ω/square, edge metalized (Figures 4-8, 4-9, bottom). As can be seen I_{gt} is still only of the order of 1mA @ -40°C while the turn-off capability has increased to 14A at the high

[1]The computer printout of static data for the devices of series 97E (standard 0.7Ω/square cathode) and of series 97H (implanted, defocused 20Ω/square cathode) is added as Appendix C.

temperature. The forward voltage drop has suffered an increase of 0.3 volts, however.

The final data line shows results for devices which were further optimized. The cathode sheet resistance was lowered from $\sim$20Ω/square to $\sim$7.0Ω/square and the epi-base resistivity was raised from $\sim$0.12Ωcm to about 0.18Ωcm. A pronounced improvement in overall electrical characteristics was achieved. The temperature range of operation was substantially extended. Turn-on was obtained with I_{gt} $\sim$0.3mA @ -60°C and turn-off capability was measured to be $I_{T\ off\ (max)}$ = 9.3A, 9.0A, and 8.5A for 25°C, 125°C, and 150°C, respectively. The maximum current that could be turned off was relatively independent of temperature.

The results show rather distinctly that Dynamic Ballasting gave very useful advantages.

V. CONCLUSION

A. High Speed-High Voltage Gate Turn-Off Device

1. The investigations of GTO-structures have shown that high speed-high voltage devices are feasible. It was demonstrated that the turn-off behavior is governed by pronounced two-dimensional effects. A narrow cathode width is of importance. Further, the introduction of an external gate series inductance and operation from a voltage source as input for turn-off will result in a safe return to the blocking state. The criteria being that:

(a) during the fall phase the second derivative of the turn-off gain d^2I_A/dI_{gq}^2 remains positive,

(b) the turn-off gain itself becomes less than unity during the tail period.

2. Further, fast turn-on t_r and fast turn-off t_f with a minimum recombination tail were simultaneously obtained through development of a special gold diffusion process. This process was critical such that:

(1) a high lifetime was designed into the active region of the device beneath the cathode emitter, and

(2) a low lifetime was build into the vicinity of the anode emitter.

3. A resultant device demonstrated switching times of 100 to 400 nanosecond and switching power capabilities of 1.55 kw @ 50kHz with 97% device efficiency. This is quite an achievement over the existing state of the art.

B. Anode Shorts and Schottky Barriers

In the available design anode shorts have been used for improvement of turn-off and reliability of the device. These anode shorts, which are placed most remote from the gate terminal, represent a non-regenerative region (or by-pass transistor) which is very effective in extinguishing the final plasma filament during turn-off. They also reduce the recombination tail. However, the turn-on is now in general impaired, especially at low temperatures.

In our research design a Schottky barrier was introduced in series with these anode shorts, which fully restored the turn-on sensitivity, while the improvement in turn-off capability due to the anode shorts was retained.

C. Dynamic Ballasting (Defocusing)

The introduction of a slightly resistive cathode and an isolated center, metalized at the edge only will have the effect of dibiasing the cathode emitter junction while the plasma is squeezed into the "geometrical center of gravity" during turn-off. During normal on-

state operation with nominal current densities a negligible additional forward voltage drop is experienced. During turn-off, however, locally high current density filaments develop because of plasma squeezing. The formation of these filaments is strongly counteracted by a lateral voltage drop in the cathode, and the exponentially dependent decrease of current injection toward the emitter center. Using this principle, the device operation was extended from -20°C to +125°C (for a conventional device) to a range of -60°C to +150°C for our research devices.

APPENDIX A

COMPUTER PROGRAM FOR PHOTO MASK SET GENERATION

The CAD artwork for the 3x3 array of test geometries (IIC, pp. 53) was generated by an "easy-to-use data-capture language" called PLOTS[75-4].

In this method geometric shapes are described as (usually opaque) polygons in a rectilinear coordinate system, either in terms of an absolute vertex location or as relative vertex coordinates in the directions left, right, top, and bottom from the previous vertex.

Thus basically, definitions D are created by a number of statements, consisting of strings of coordinates. These definitions may be placed in certain locations by "Q"-calls and are organized to appear on a specified photo mask M.

The PLOTS programs will then interface with either automatic-drafting equipment and CRT display systems for error checking and testing, or they will through an intermediate conversion serve to control a precision photoplotter for mask set fabrication.

In Figure A-1 is shown a sample PLOTS language statement (top), which is translated into the corresponding computer generated artwork (bottom).

```
10 M1
20 O X2.8Y12 R1.6 T.5 L.6 T.5 L1 B1 ;FIGURE 1
30 O X6.2Y5 T.6 L.4 T.4 R1 T1 R1 B2 L.5 T.6 L.5 B.6 L.6 ;FIGURE2
40 P X8.8Y14.8 R1.6 B1.6 L1 TO X8.8Y13.6 T1.2 ;FIGURE 3
50 P X2.8Y5 TO X3.3 TO X3.8Y5.5 TO X4.3 TO X4.8Y5S
60 TO X5.3 TO Y6.6 TO X3.7 TO X2.8Y5.6 TO Y5 ;FIGURE 3A
70 W .4
80 L X7.8 Y4.4 TO X8.2 TO X8.6Y4.8 TO Y7 ;FIGURE 4
90 D1 XOYO ;DEFINITION 1
100 M1
110 P X1.2Y0 R.5 T1.6 L1.5 B.6 TO X1.2Y0 ;FIGURE 6
120 W .4
130 L X2.6 Y0 T1.6 TO X2.2Y2 TO X0 ;FIGURE 7
140 E ;END OF DEFINITION
150 O 1 X2.8Y7.5 ;PLACES FIGURE 5 AT FIGURE 8
160 O 1 X8.8Y10 ROTATE 2 ;PLACES FIGURE 5 AS FIGURE 9
170 O 10095 X6.8Y13.1 ;PLACES FIGURE 16 AS FIGURE 10
180 OE X1.4Y5 TO X10.4 TO Y12.4 L4.4 T2 L4.6 TO Y5 ;FIGURE 11
190 OH X7.4Y4 TO X9.4 T7.4 L2 R1 L2.5 T5 L2.5 TO Y4 ;FIGURE 12
200 OE X6.8Y.8 TO X9.8 T1.6 L5 H1.6 ;FIGURE 14
210 OH X7.2 Y1.2 T.8 R2.2 R.8 L2.2 ;FIGURE 15
220 O X1.8Y.9 H1 T1 L.5 T.5 L.5 B1.5 AND 2R1.5 ;FIGURES 15,15A,15B
```

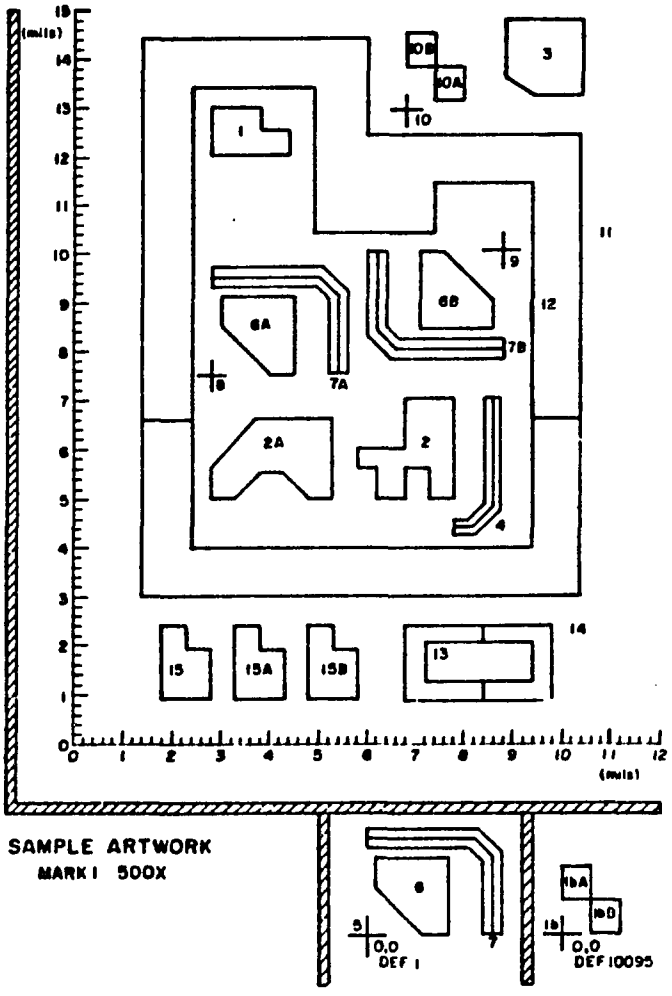


FIGURE A-1 SAMPLE PLOTS LANGUAGE STATEMENT (TOP) AND COMPUTER GENERATED ARTWORK (BOTTOM). THE "FIGURE" NUMBERS THAT FOLLOW THE PLOTS STATEMENTS (SEPARATED BY SEMICOLONS) CORRESPOND TO NUMBERED SHAPES ON THE ARTWORK (AFTER B.J. Korenjak 74-1)

Figure A-2 is the program defining the photo mask set which was used to fabricate the test devices described in Chapter III, and IVB.

For illustration purposes let us follow the steps that will generate the cathode emitter mask pattern of Device 3 (Figure 3-6, pp. 54 or Figure B-16, pp. 147, bottom left).

First a single site, D24 is defined by the statement

P XO Y-2.25 (R_{ight} 16 T_{op} 1) T2.5 (L_{eft} 16 T1) B_{ottom} 4.5 (line 1940)

Then in D25 (line 1960 to 2040) the first quadrant of the pattern is generated with the center of the (whole) pattern being the origin (fiducial point). Q calls place the single sites into the proper locations, create more of them by "and" statements (ex. line 1990) or rotate them, as done to get the vertical site close to the center (Q24 X4.75Y14R_{otate} 3, line 1970).

In D65 the quarter pattern is assigned to its mask level M3 (line 5320-5330) and stacked up with all other quarter patterns belonging to Device 3.

In D73 (line 6130) the cathode pattern is rotated and mirrored simultaneously with its 1st quadrant companions of the other masks such that all 4 quadrants (i.e., the entire pattern now exists).

Finally, the call Q73 (line 6360) will place the cathode sites and all other mask levels into the lower left hand corner of the array of devices (called out as Q68 to Q75 (line 6310 to line 6380).

```
U      1 X.5Y6
W      1.0500 ; CIRCLE DIAMETER          8.0000
L X     4.0000 Y     0.0     TO X    -4.0000 Y     0.0
L X     3.8637 Y     1.0353  TO X    -3.8637 Y    -1.0353
L X     3.4641 Y     2.0000  TO X    -3.4641 Y    -2.0000
L X     2.8284 Y     2.8284  TO X    -2.8284 Y    -2.8284
L X     2.0000 Y     3.4641  TO X    -2.0000 Y    -3.4641
L X     1.0353 Y     3.8637  TO X    -1.0353 Y    -3.8637
L X     0.0000 Y     4.0000  TO X    -0.0000 Y    -4.0000
L X    -1.0353 Y     3.8637  TO X     1.0353 Y    -3.8637
L X    -2.0000 Y     3.4641  TO X     2.0000 Y    -3.4641
L X    -2.8284 Y     2.8284  TO X     2.8284 Y    -2.8284
L X    -3.4641 Y     2.0000  TO X     3.4641 Y    -2.0000
L X    -3.8637 Y     1.0353  TO X     3.8637 Y    -1.0353
E
D2 X0Y0; P+ DIFF TP1
U X15Y12 R12 T53 L12 R33 L2 B17 R2 B3
U X53Y-1 R12 T62 L4 T4 L8 B66
Q1 X61Y61
E
D3 X0Y0; P+ DIFF TD1
P X-1Y32 R13 B3 (B14 R2) R2 B3 R10$
T3 (T39 R2) T3 R24 B3 (B39 R2) B16 $
R11 T66 (T4 L4) L62 B33
Q1 X61Y61
E
D4 X0Y0; P+ DIFF TP2
W4
L X9 Y15 T50
L X27Y11 T54 AND 1R18
L X63Y-1 T62
Q1 X61Y61
E
D5 X0Y0; P+ DIFF TD2
P X-1Y32 R7.5 B3 (B12 R1) B2 R3 T2 (T37 R1) T4 L12.5 B26
P X25.5 Y11 R3 T2 (T4) R1) T4 L5 B4 (B37 R1)B6
P X43.5Y11 R3 T2 (T41 R1) T4L5 B4(B41 R1)B2
P X61.5Y-1 R3.5 T62 L4.5 B7 (B41 R1) B14
O X-1Y57 R62 T8 L62 B8
Q1 X61Y61
E
D6 X0Y0; P+ DIFF TP3
W2
L X0Y14 T25 AND 1R9.5
L X14Y11 R17
L X8.5Y20.5 R22.5 AND 3T9.5
L X-1Y39.5 R13 AND 1T9.5
L X43Y0 R22 AND 1T9.5
L X42Y19 R23 AND 1T9.5
L X41Y36 R24 AND 1T9.5
O X-1Y57.5 R62 T7.5 L62 B7.5
O X-1Y56 R24 T5 L24 B5
Q1 X61Y61
E
D7 X0Y0; P+ DIFF TD3
P X-0.5Y14 R1 (T16 R1) T2 R0.5 B2 (B16 R1) R4 B4 R18 T1.5$
(L14T1) L2 T4.5 L2 T48 L13.5 B51
P X43Y-0.5 (R16 B1) R0 T3 L0 (L16 B1) B1 AND 1T9.5
P X65Y17.5 T3 L7 (L16 B1) B1 R1 (R16 B1) R0
```

A-2a CAD PROGRAM, PAGE 1 OF 14

A-2 COMPUTER PROGRAM (PLOTS LANGUAGE) FOR ARTWORK GENERATION TO PRODUCE PHOTOMASK SET FOR 3 x 3 ARRAY OF GTO-DEVICES; LINE 10-8020, 14 PAGES (SEE APPENDIX B AND FIGURE 3-6).

```
P X65 Y27 T3 L7 (L16 B1) B1 (R16 B1) R7                                  00000610
P X65 Y30.5 T3 L8 (L16 B1) B1 R1(R16 B1) R7                              00000620
P X65 Y46 T3 L8 (L16 B1) B1 (R16 B1) R8                                  00000630
P X31 Y20 T1 (L16 T1) L3 B3 R5 (R14 T1)                                  00000640
P X31 Y29.5 T1 (L16 T1) L3 B3 R3 (R16 T1) AND 2T9.5                      00000650
P X-1 Y57 R16 (R16 T1) R10 B1.5 (R16 B1) R8 T5.5 (L4 T4) L02 B8          00000660
O X61 Y-1 T18.5 L1 T22 L1 T21.5 R6 B02 L4                                00000661
Q1 X61 Y61                                                               00000670
E                                                                        00000680
D8 X0 Y0; P+ DIFF TP4                                                    00000690
W 1.2                                                                    00000700
L X0Y13.5 T20.4AND 2R5.8                                                 00000710
L X13 Y10.1 R18.5                                                        00000720
L X11 Y15.9 R20.5 AND 2T5.8                                              00000730
L X-1 Y33.3 R32.5 AND 4T5.8                                              00000740
L X42.5 Y0 R22.5 AND 3T5.8                                               00000750
L X41.5 Y23.2 R23.5 AND 2T5.8                                            00000760
L X40.5 Y40.6 R24.5 AND 3T5.8                                            00000770
O X-1 Y55.9 R32.5 T1.5 R33.5 T3.6 L4 T4 L02 B9.1                         00000780
Q1 X61 Y61                                                               00000790
E                                                                        00000800
D9 X0 Y0; P+ DIFF TD4                                                    00000810
P X-0.3 Y13.5 R0.6 (T17 R0.6) T3.7 L1.8 B3.7 (B17 R0.6) AND$             00000820
2R5.8                                                                    00000830
P X11.6 Y15 R4.9 (R15.5 T0.6) T0.6 (L17 T0.6) L2.9 B1.8                  00000840
P X11.6 Y20.8 R2.9 (R17 T0.6) T0.6 (L17 T0.6) L2.9$                      00000850
B1.8 AND 6T5.8                                                           00000860
P X42.5 Y-0.3 (R17 B0.6) R3.5 T1.8 L5.5 (L17 B0.6)B3.6 AND$              00000870
3T5.8                                                                    00000880
P X41.5 Y22.9 R1 (R17 B0.6) R3.5 T1.8 L6.5 (L17 B0.6) B0.6               00000890
P X41.5 Y28.7 (R17 B0.6) R6.5 T1.8 L6.5 (L17 B0.6)B0.6$                  00000900
AND 11B.8                                                                00000910
P X40.5 Y49.3 R1 (R17 B0.6) R6.5 T1.8 L7.5 (L17 B0.6) B0.6               00000920
P X40.5 Y46.1 (R17 B0.6) R7.5 T1.8 L7.5 (L17 B0.6) B0.6 AND$             00000930
2T5.8                                                                    00000940
P X-1 Y32 R12.6 B18.5 R14.4 B4 R18.5 T0.4 (L15.5 T0.6) L1.2$             00000950
T4.9 L1.5 T41.1 L14 B25                                                  00000960
O X-1 Y56.5 R32.5 T1.2 R33.5 T3.3 L4 T4 L02 B8.5                         00000970
O X61 Y6 R4 T25 L4 B25                                                   00000980
O X60 Y24.1 R5 T19 L5 B19                                                00000990
O X59 Y41.5 R6 T17.5 L6 B17.5                                            00001000
Q1 X61 Y61                                                               00001010
E                                                                        00001020
D10 X0Y0; P+ DIFF T2 TP1 NEG                                             00001030
W8                                                                       00001040
L X0Y9 T26                                                               00001050
L X40 Y9 T51                                                             00001060
E                                                                        00001070
D11 X0 Y0; P+ DIFF T2 TD1 NEG                                            00001080
P X-1 Y9 R6 T6 (T14 L2) T6 L4 B26                                        00001090
P X35 Y9 R10 T6 (T39 L2) T6 L6 B6 (B39 L2) B6                            00001106
E                                                                        00001110
D12 X0 Y0; P+ DIFF T2 TP2 NEG                                            00001120
W4                                                                       00001130
L X0 Y12 T22                                                             00001140
L X18 Y12 T47                                                            00001150
L X36 Y8 T51 AND IR18                                                    00001160
E                                                                        00001170
D13 X0 Y0; P+ DIFF T2 TD2 NEG                                            00001180
```

A2-2 CAD PROGRAM, PAGE 2 OF 14

A-2 COMPUTER PROGRAM (PLOTS LANGUAGE) FOR ARTWORK GENERATION TO PRODUCE PHOTOMASK SET FOR 3 x 3 ARRAY OF GTO-DEVICES; LINE 10-8020, 14 PAGES (SEE APPENDIX B AND FIGURE 3-6).

```
P X-1 Y12 R3.5 T5 (T12 L1)T5 L2.5 B32                                00001190
P X 15.5 Y12 R5 T5 (T37 L1) T5 L3 B5 (B37 L1) B5                     00001200
P X33.5 Y8 R5 T5 (T41 L1) T5 L3 B5 (B41 L1) B5 AND 1R18              00001210
E                                                                    00001220
D14 X0 Y0; P+ DIFF T2 TP3 NEG                                        00001230
W2.5                                                                 00001240
L X4.75 Y10 T24                                                      00001250
L X35 Y15.75 L22                                                     00001260
L X35 Y25.25 L24 AND 3T9.5                                           00001270
L X34 Y4.75 R24 AND 1T9.5                                            00001280
L X38 Y23.75 R24 AND 1T9.5                                           00001290
L X37 Y42.75 R24 AND 1T9.5                                           00001300
E                                                                    00001310
D15 X0 Y0; P+ DIFF T2 TD3 NEG                                        00001320
P X3 Y10 R3.5 T4 (T16 L1) T4 L1.5 B4 (B16 L1)B4                      00001330
P X35 Y14 T3.5 L4 (L14 B1) L4 B1.5 R4 (R14 B1) R4                    00001340
P X35 Y23.5 T3.5 L4 (L16 B1) L4 B1.5 R4 (R16 B1) R4 AND$             00001350
3T9.5                                                                00001360
P X39 Y3 R4 (R16 T1) R4 T1.5 L4 (L16 T1) L4 B3.5 AND$                00001370
1T9.5                                                                00001380
P X28 Y22 R4 (R16 T1) R4 T1.5 L4 (L16 T1) L4 B3.5 AND$               00001390
1T9.5                                                                00001400
P X37 Y41 R4 (R16 T1) R4 T1.5 L4 (L16 T1) L4 B3.5 AND$               00001410
1T9.5                                                                00001420
E                                                                    00001430
D16 X0Y0; P+ DIFF T2 TD4 NEG                                         00001440
W2                                                                   00001450
L X2.4 Y10.5 T23 AND 1R5.8                                           00001460
L X13 Y13 R21.5                                                      00001470
L X11.5 Y18.8 R23 AND 6T5.8                                          00001480
L X39.5 Y2.9 R23 AND 3T5.8                                           00001490
L X38.5 Y26.1 R23 AND 2T5.8                                          00001500
L X37.5 Y43.5 R23 AND 2T5.8                                          00001510
E                                                                    00001520
D17 X0Y0; ANDUE SHORT TD4, SINGLE SIFt                               00001530
P X0 Y-1.3 R3 (R17 T0.8)R3 T1.4 L3 (L17 T0.8) L3 B2.8                00001540
E                                                                    00001550
D18 X0Y0; P+ DIFF T2 TD4 NEG                                         00001560
Q17 X2.9 Y10.5 R3 AND 1R5.8                                          00001570
P X34.5 Y11.7 L3 (L15.5 T0.8) L3 T1.4 R3 (R15.5 T0.8)                00001580
R3 B2.8                                                              00001590
Q17 X34.5 Y18.8 R2 AND 6T5.8                                         00001600
Q17 X39.5 Y2.9 AND 3T5.8                                             00001610
Q17 X38.5 Y26.1 AND 2T5.8                                            00001620
Q17 X37.5 Y43.5 AND 2T5.8                                            00001630
E                                                                    00001640
D19 X0Y0; N+ DIFF TP1                                                00001650
O X-1 Y15 R11 T14 L11 B14                                            00001660
O X30 Y15 R20 T39 L20 B39                                            00001670
E                                                                    00001680
D20 X0 Y0; N+ DIFF TD1                                               00001690
P X-1 Y15 R12 (T14 L2) L10 B14                                       00001700
P X29 Y15 R22 (T39 L2) L10 (B39 L2)                                  00001710
E                                                                    00001720
D21 X0Y0; N+ DIFF TP2                                                00001730
W8                                                                   00001740
L X0 Y17 T12                                                         00001750
L X18 Y17 T37                                                        00001760
L X36 Y13 T41 AND 1R18                                               00001770
```

A2-3 CAD PROGRAM, PAGE 3 OF 14

A-2 COMPUTER PROGRAM (PLOTS LANGUAGE) FOR ARTWORK GENERATION TO PRODUCE PHOTOMASK SET FOR 3 x 3 ARRAY OF GTO-DEVICES; LINE 10-8020, 14 PAGES (SEE APPENDIX B AND FIGURE 3-6).

```
E                                                                    00001780
D22 X0Y0; N+ DIFF TD2                                                00001790
P X-1 Y17 R5.5 (T12 L1) L4.5 B12                                     00001800
P X13.5 Y17 R9 (T37 L1) L7 (B37 L1)                                  00001810
P X31.5 Y13 R9 (T41 L1) L7 (B41 L1) AND IR16                         00001820
E                                                                    00001830
D23 X0Y0; N+ DIFF TP3                                                00001840
M 3.5                                                                00001850
L X4.75 Y14 T16                                                      00001860
L X31 Y15.75 L14                                                     00001870
L X31 Y25.25 L16 AND 3T9.5                                           00001880
L X43 Y4.75 R16 AND 1T9.5                                            00001890
L X42 Y23.75 R16 AND 1T9.5                                           00001900
L X41 Y42.75 R16 AND 1T9.5                                           00001910
E                                                                    00001920
D24 X0Y0; CATHODE TD3, SINGLE SIDE                                   00001930
P X0 Y-2.25 (R16 T1) T2.5 (L16 T1) B4.5                              00001940
E                                                                    00001950
D25 X0Y0; N+ DIFF TD3                                                00001960
Q24 X4.75 Y14 R3                                                     00001970
P X31 Y13.5 (L14 T1) T2.5 (R14 T1) B4.5                              00001980
Q24 X31 Y25.25 R2 AND 3T9.5                                          00001990
Q24 X43 Y4.75 AND 1T9.5                                              00002000
Q24 X42 Y23.75 AND 1T9.5                                             00002010
Q24 X41 Y42.75 AND 1T9.5                                             00002020
E                                                                    00002030
D26 X0Y0; N+ DIFF TP4                                                00002040
M1.6                                                                 00002050
L X2.9 Y13.5 T17 AND 1R5.8                                           00002060
L X16 Y13 R15.5                                                      00002070
L X14.5 Y18.8 R17 AND 6T5.8                                          00002080
L X42.5 Y2.9 R17 AND 3T5.8                                           00002090
L X41.5 Y20.1 R17 AND 2T5.8                                          00002100
L X 40.5 Y43.5 R17 AND 2T5.8                                         00002110
E                                                                    00002120
D27 X0Y0; CATHODE TD4, SINGLE SIDE                                   00002130
P X0 Y-1.1 (R17 T0.6) T1 (L17 T0.6) B2.2                             00002140
E                                                                    00002150
D28 X0Y0; N+ DIFF TD4                                                00002160
Q27 X2.9 Y13.5 R3 AND 1R5.8                                          00002170
P X31.5 Y11.9 (L15.5 T0.6) T1 (R15.5 T0.6)B2.2                       00002180
Q27 X31.5 Y18.8 R2 AND 6T5.8                                         00002190
Q27 X42.5 Y2.9 AND 3T5.8                                             00002200
Q27 X41.5 Y20.1 AND 2T5.8                                            00002210
Q27 X40.5 Y43.5 AND 2T5.8                                            00002220
E                                                                    00002230
D29 X0Y0; CONTACT OPEN TP1                                           00002240
Q2 X0Y0                                                              00002250
O X-0.5 Y15.5 R10 T13 L10 B13                                        00002260
O X30.5 Y15.5 R19 T38 L19 B38                                        00002270
E                                                                    00002280
D30 X0Y0; CONTACT OPEN TP1, DEFOCUS                                  00002290
Q2 X0Y0                                                              00002300
M7                                                                   00002310
L X6 Y15.5 T13                                                       00002320
L X34 Y15.5 T38 AND 1R12                                             00002330
E                                                                    00002340
D31 X0Y0; CONTACT OPEN TD1                                           00002350
Q3 X0Y0                                                              00002360
```

A2-4 CAD PROGRAM, PAGE 4 OF 14

A-2 COMPUTER PROGRAM (PLOTS LANGUAGE) FOR ARTWORK GENERATION TO PRODUCE PHOTOMASK SET FOR 3 x 3 ARRAY OF GTO-DEVICES; LINE 10-8020, 14 PAGES (SEE APPENDIX B AND FIGURE 3-6).

```
P X-0.5 Y15.5 R11 (T13 L2) L9 B13                                00002370
P X29.5 Y15.5 R21 (T38 L2) L17 (B38 L2)                          00002380
E                                                                00002390
D32 XOYO; CONTACT OPEN TD1, DEFOCUS                              00002400
U3 XOYO                                                          00002401
P X3.5 Y15.5 R7(T13 L2)$                                         00002410
L7 (B13 R2)                                                      00002420
P X29.5 Y15.5 R7 (T38 R2) L7 (B38 L2)                            00002430
P X50.5 Y15.5 L7 (T38 L2) R7 (B38 R2)                            00002440
E                                                                00002450
D33 XOYO; CONTACT OPEN TP2                                       00002460
U4 XOYO                                                          00002470
W7.4                                                             00002480
L X0 Y17.3 T11.4                                                 00002490
L X18 Y17.3 T36.4                                                00002500
L X36 Y13.3 T40.4 AND IR18                                       00002510
E                                                                00002520
D34 XOYO; CONTACT OPEN TP2, DEFOCUS                              00002530
U4 XOYO                                                          00002540
W2.2                                                             00002550
L X2.6 Y17.3 T11.4                                               00002560
L X20.6 Y17.3 T36.4 AND IL5.2                                    00002570
L X38.6 Y13.3 T40.4 AND IL5.2                                    00002580
L X56.6 Y13.3 T40.4 AND IL2.2                                    00002590
E                                                                00002600
D35 XOYO; CONTACT OPEN TD2                                       00002610
U5 XOYO                                                          00002620
P X-0.7 Y17.3 R4.9 (T11.4 L1) L3.9 B11.7                         00002630
P X13.8 Y17.3R8.4 (T36.4 L1) L6.4 (B36.4 L1)                     00002640
P X31.8 Y13.3 R8.4 (T40.4 L1) L6.4 (B40.4 L1)AND IR18            00002650
E                                                                00002660
D36 XOYO; SINGLE CATHODE TD2 DFC                                 00002670
W2.2                                                             00002680
L X-3.1 Y0 (T40.4 R1)                                            00002690
L X3.1 Y0 (T40.4 L1)                                             00002700
E                                                                00002710
D37 XOYO; CONTACT OPEN TD2, DEFOCUS                              00002720
U5 XOYO                                                          00002730
W2.2                                                             00002740
L X3.1 Y17.3 (T11.4 L1)                                          00002750
L X14.9 Y17.3 (T36.4 R1)                                         00002760
L X21.1 Y17.3 (T36.4 L1)                                         00002770
U36 X36 Y13.3 AND IR18                                           00002780
E                                                                00002790
D38 XOYO; CONTACT OPEN TP3                                       00002800
U6 XOYO                                                          00002810
W3.1                                                             00002820
L X4.75Y14.2 T15.6                                               00002830
L X30.8 Y15.75 L15.6                                             00002840
L X30.8Y25.25 L15.6 AND 3T9.5                                    00002850
L X43.2Y4.75R15.6 AND 1T9.5                                      00002860
L X42.2Y25.75 R15.6 AND 1T9.5                                    00002870
L X41.2 Y42.75 R15.6 AND 1T9.5                                   00002880
E                                                                00002890
D39 XOYO; SINGLE CATHODE TP3 DFC                                 00002900
M1                                                               00002910
LX0Y-1 R15.5 AND IT2                                             00002920
E                                                                00002930
D40 XOYO; CONTACT OPEN TP3 DEFOCUS                               00002940
```

A2-5 CAD PROGRAM, PAGE 5 OF 14

A-2 COMPUTER PROGRAM (PLOTS LANGUAGE) FOR ARTWORK GENERATION TO PRODUCE PHOTOMASK SET FOR 3 x 3 ARRAY OF GTO-DEVICES; LINE 10-8020, 14 PAGES (SEE APPENDIX B AND FIGURE 3-6).

```
Q6 X0Y0                                                                 00002950
Q39 X4.75 Y14.25 R3                                                     00002960
Q39 X30.75Y25.25 R2 AND 3T9.5                                           00002970
Q39 X43.25Y4.75 AND 1T9.5                                               00002980
Q39 X42.25Y23.75 AND 1T9.5                                              00002990
Q39 X41.25Y42.75 AND 1T9.5                                              00003000
W1                                                                      00003010
L X30.75Y14.75 L13.5 AND 112                                            00003020
E                                                                       00003030
D77 X0Y0; SINGLE CATHODE TD3                                            00003040
P X0Y-2 (R15.5T1) T2 (L15.5T1) B4                                       00003050
E                                                                       00003060
D41 X0Y0; CONTACT OPEN TD3                                              00003070
Q7 X0Y0                                                                 00003080
Q77 X4.75Y14.25 R3                                                      00003090
P X30.75Y13.75 (L13.5T1) T2 (R13.5T1) B4                                00003100
Q77 X30.75Y25.25 R2 AND 3T9.5                                           00003110
Q77 X43.25Y4.75 AND 1T9.5                                               00003120
Q77 X42.25Y23.75 AND 1T9.5                                              00003130
Q77 X41.25Y42.75 AND 1T9.5                                              00003140
E                                                                       00003150
D42 X0Y0 ; SINGLE CATHODE TD3 DFC                                       00003160
W1                                                                      00003170
L X0Y-1.5 (R15.5T1)                                                     00003180
L X0Y1.5 (R15.5B1)                                                      00003190
E                                                                       00003200
D43 X0Y0; CONTACT OPEN TD3 DEFOCUS                                      00003210
Q7 X0Y0                                                                 00003211
Q42 X4.75Y14.25 R3                                                      00003220
Q42 X30.75Y25.25 R2 AND 3T9.5                                           00003230
Q42 X43.25Y4.75 AND 1T9.5                                               00003240
Q42 X42.25Y23.75 AND 1T9.5                                              00003250
Q42 X41.25Y42.75 AND 1T9.5                                              00003260
W1                                                                      00003270
L X30.75Y14.25 (L13.5T1)                                                00003280
L X30.75Y17.25 (L13.5B1)                                                00003290
E                                                                       00003300
D44 X0Y0; SINGLE CATHODE TP4                                            00003310
W1.4                                                                    00003320
L X0Y0   R16.8                                                          00003330
E                                                                       00003340
D45 X0Y0; CONTACTOPEN TP4                                               00003350
Q8 X0Y0                                                                 00003360
Q44 X2.9Y13.6 R3 AND 1R5.8                                              00003370
W1.4                                                                    00003380
L X16.1Y13 R15.3                                                        00003390
Q44 X31.4Y18.8 R2 AND 6T5.8                                             00003400
Q44 X42.6Y2.9 AND 3T5.8                                                 00003410
Q44 X41.6Y26.1 AND 2T5.8                                                00003420
Q44 X40.6Y43.5 AND 2T5.8                                                00003430
E                                                                       00003440
D 46 X0Y0; SINGLE CATHODE TP4 DFC                                       00003450
W0.5                                                                    00003460
L X0 Y-0.45 R16.8 AND 110.9                                             00003470
E                                                                       00003480
D47 X0Y0; CONTACT OPEN TP4 DEFOCUS                                      00003490
Q8 X0Y0                                                                 00003500
Q46 X2.9 Y13.6 R3 AND 1R5.8                                             00003510
W0.5                                                                    00003520
```

A2-6 CAD PROGRAM, PAGE 6 OF 14

A-2 COMPUTER PROGRAM (PLOTS LANGUAGE) FOR ARTWORK GENERATION TO PRODUCE PHOTOMASK SET FOR 3 x 3 ARRAY OF GTO-DEVICES; LINE 10-8020, 14 PAGES (SEE APPENDIX B AND FIGURE 3-6).

```
L X16.1 Y12.55 R15.3 AND 1T0.9                                  00003530
Q46 X31.4 Y18.8 R2 AND 6T5.8                                    00003540
Q46 X42.6 Y2.9 AND 3T5.8                                        00003550
Q46 X41.6 Y26.1 AND 2T5.8                                       00003560
Q46 X40.6 Y43.5 AND 2T5.8                                       00003570
E                                                               00003580
D48 XOYO; SINGLE CATHODE TD4                                    00003590
P X0 Y-1 (R16.8 T0.6) T0.8 (L16.8 T0.6) B2                      00003600
E                                                               00003610
 D49 XOYO; CONTACT OPEN TD4                                     00003620
Q9 XOYO                                                         00003630
Q48 X2.9 Y13.6 R3 AND 1R5.8                                     00003640
P X31.4 Y12 (L15.3 T0.6) T0.8 (R15.3 T0.6) B2                   00003650
Q48 X31.4 Y18.8 R2 AND 6T5.8                                    00003660
Q48 X42.6 Y2.9 AND 3T5.8                                        00003670
Q48 X41.6 Y26.1 AND 2T5.8                                       00003680
Q48 X40.6 Y43.5 AND2T5.8                                        00003690
E                                                               00003700
D50 XOYO; SINGLE CATHODE TD4, DFL                               00003710
H0.5                                                            00003720
L X0 Y-0.75 (R16.8 T0.6)                                        00003730
L X0 Y0.75      (R16.8 B0.6)                                    00003740
E                                                               00003750
D51 XOYO; CONTACT OPEN TD4, DEFOCUS                             00003760
Q9 XOYO                                                         00003770
Q50 X2.9 Y13.6 R3 AND 1R5.8                                     00003780
H0.5                                                            00003790
L X31.4 Y12.25 (L15.4 T0.6)                                     00003800
L X31.4 Y13.75 (L15.4 B0.6)                                     00003810
Q50 X31.4 Y18.8 R2 AND 6T5.8                                    00003820
Q50 X42.6 Y2.9 AND 3T5.8                                        00003830
Q50 X41.6 Y26.1 AND 2T5.8                                       00003840
Q50 X40.6 Y43.5 AND 2T5.8                                       00003850
E                                                               00003860
D52 XOYO; METAL TP1 NEG                                         00003870
U X-1 Y-1 R13 T13 L13 B13                                       00003880
O X11 Y-1 R38.5 T16.7 L19 B6.7 L19.5 B10                        00003890
O X-1 Y11 R10.5 T4.7 L10.5 B4.7                                 00003900
Q29 XOYO                                                        00003910
O X-1 Y32 R17 T33 L17 B33                                       00003920
O X26 Y57 R26 T8 L26 B8                                         00003930
E                                                               00003940
D53 XOYO; METAL TD1 NEG                                         00003950
O X-1 Y-1 R13 T13 L13 B13                                       00003960
O X11 Y-1 R39.5 T16.7 L21 B6.7 L18.5 B10                        00003970
Q31 XOYO                                                        00003980
O X-1 Y11 R11.5 T4.7 L11.5 B4.7                                 00003990
E                                                               00004000
D54 XOYO; METAL TP2 NEG                                         00004010
O X-1 Y-1 R13 T9 L11.5 T4 L11.5 B13                             00004020
O X11 Y-1 R40.7 T9 L46.7 B9                                     00004030
O X-1 Y11 R4.7 T6.5 L4.7 B6.5                                   00004040
H7.4                                                            00004050
L X18 Y7.7 T9.8                                                 00004060
L X36 Y7.7 T5.8 AND 1R18                                        00004070
Q33 X0 Y0                                                       00004080
O X-1 Y32 R9 T35 L9 B33                                         00004090
O X-1 Y57 R62 T8 L62 B8                                         00004100
E                                                               00004110
```

A2-7 CAD PROGRAM, PAGE 7 OF 14

A-2 COMPUTER PROGRAM (PLOTS LANGUAGE) FOR ARTWORK GENERATION TO PRODUCE PHOTOMASK SET FOR 3 x 3 ARRAY OF GTO-DEVICES; LINE 10-8020, 14 PAGES (SEE APPENDIX B AND FIGURE 3-6).

```
D55 XOYO; METAL TU2 NEG                                          00004120
O X-1 Y-1 R13 T9 L1.5 T4 L11.5 B13                               00004130
O X11 Y-1 R47.2 T9 L47.2 B9                                      00004140
O X-1 Y11 R5.2 T6.5 L5.2 B6.5                                    00004150
W8.4                                                             00004160
L X18 Y7.7 T9.8                                                  00004170
L X36 Y7.7 T5.8 AND 1R18                                         00004180
Q35 XOYO                                                         00004190
E                                                                00004200
D56 XOY8; METAL TP3 NEG                                          00004210
O X-1 Y-1 R13 T9 L1 T4 L12 B13                                   00004220
O X11 Y-1 R30 T17 L1 T19 L1 T20.3 L6 B47.3 L22 B9                00004240
W3.1                                                             00004240
L X4.75 Y11.8 T2.5                                               00004250
L X33.2 Y15.75 L2.5 AND 4T9.5                                    00004260
L X40.6 Y4.75 R2.5 AND 1T9.5                                     00004270
L X39.8 Y23.75 R2.5 AND 1T9.5                                    00004280
L X38.8 Y42.75 R2.5 AND 1T9.5                                    00004290
Q38 XOYO                                                         00004300
O X-1 Y32 R14 T26 L14 B26                                        00004310
O X10 Y32.5 B18.5 R3 B4 R2 T7 L2 T15.5 L3                        00004320
O X61 Y-1 T21 L1 T19 L1 T19 R6 B59 L4                            00004330
E                                                                00004340
D57 XOYO; METAL TU3 NEG                                          00004350
O X-1 Y-1 R13 T9 L1.5 T4 L11.5 B13                               00004360
O X11 Y-1 R30 T17.5 L1 T19.5 L1 T19.8 L6 B47.8 L22 B9            00004370
W4.1                                                             00004380
L X4.75 Y11.8 T2.5                                               00004390
L X33.2 Y15.75 L2.5 AND 4T9.5                                    00004400
L X40.8 Y4.75 R2.5 AND 1T9.5                                     00004410
L X39.8 Y23.75 R2.5 AND 1T9.5                                    00004420
L X38.8 Y42.75 R2.5 AND 1T9.5                                    00004430
Q41 XOYO                                                         00004440
E                                                                00004450
D58 XOYO; METAL TP4 NEG                                          00004460
O X-1 Y-1 R13 T9 L0.5 T4 L12.5 B13                               00004470
O X11 Y-1 R30 T22.1 L1 T17.6 L1 T17.2 L6 B47.9 L22 B9            00004480
W1.4                                                             00004490
L X2.9 Y11.9 T1.8 AND 1R5.8                                      00004500
L X33.1 Y13 L1.8 AND 7T5.8                                       00004510
L X40.9 Y2.9 R1.8 AND 3T5.8                                      00004520
L X39.9 Y26.1 R1.8 AND 2T5.8                                     00004530
L X38.9 Y43.5 R1.8 AND 2T5.8                                     00004540
Q45 XOYO                                                         00004550
O X-1 Y32 R14 T26 L14 B26                                        00004560
O X11 Y32.5 B19 R2 B4 R1.5 T5.8 L1.5 T17.2 L2                    00004570
O X61 Y-1 T24.8 L1 T17.4 L1 T17.8 R6 B60 L4                      00004580
E                                                                00004590
D59 XOYO; METAL TU4 NEG                                          00004600
O X-1 Y-1 R13 T9 L0.5 T4 L12.5 B13                               00004610
O X11 Y-1 R30 T22.4 L1 T17.6 L1 T17.2 L6 B48.2 L22 B9            00004620
W2                                                               00004630
L X2.9 Y11.9 T1.8 AND 1R5.8                                      00004640
L X33.1 Y13 L1.8 AND 7T5.8                                       00004650
L X40.9 Y2.9 R1.8 AND 3T5.8                                      00004660
L X39.9 Y26.1 R1.8 AND 2T5.8                                     00004670
L X38.9 Y43.5 R1.8 AND 2T5.8                                     00004680
Q49 XOYO                                                         00004690
E                                                                00004700
```

A2-8 CAD PROGRAM, PAGE 8 OF 14

A-2 COMPUTER PROGRAM (PLOTS LANGUAGE) FOR ARTWORK GENERATION TO PRODUCE PHOTOMASK SET FOR 3 x 3 ARRAY OF GTO-DEVICES; LINE 10-8020, 14 PAGES (SEE APPENDIX B AND FIGURE 3-6).

```
D60 X0Y0; P1                                00004710
M1                                          00004720
Q2 X0Y0                                     00004730
M2                                          00004740
Q10 X0Y0                                    00004750
M3                                          00004760
Q19 X0Y0                                    00004770
M4                                          00004780
Q29 X0Y0                                    00004790
M5                                          00004800
Q30 X0Y0                                    00004810
M7                                          00004820
Q52 X0Y0                                    00004830
E                                           00004840
D61 X0Y0; D1                                00004850
M1                                          00004860
Q3 X0Y0                                     00004870
M2                                          00004880
Q11 X0Y0                                    00004890
M3                                          00004900
Q20 X0Y0                                    00004910
M4                                          00004920
Q31 X0Y0                                    00004930
M5                                          00004940
Q32 X0Y0                                    00004950
M7                                          00004960
Q53 X0Y0                                    00004970
E                                           00004980
D62 X0Y0; P2                                00004990
M1                                          00005000
Q4 X0Y0                                     00005010
M2                                          00005020
Q12 X0Y0                                    00005030
M3                                          00005040
Q21 X0Y0                                    00005050
M4                                          00005060
Q33 X0Y0                                    00005070
M5                                          00005080
Q34 X0Y0                                    00005090
M7                                          00005100
Q54 X0Y0                                    00005110
E                                           00005120
D63 X0Y0; D2                                00005130
M1                                          00005140
Q5 X0Y0                                     00005150
M2                                          00005160
Q13 X0Y0                                    00005170
M3                                          00005180
Q22 X0Y0                                    00005190
M4                                          00005200
Q35 X0Y0                                    00005210
M5                                          00005220
Q37 X0Y0                                    00005230
M7                                          00005240
Q55 X0Y0                                    00005250
E                                           00005260
D64 X0Y0; P3                                00005270
M1                                          00005280
Q6 X0Y0                                     00005290
```

A2-9 CAD PROGRAM, PAGE 9 OF 14

A-2 COMPUTER PROGRAM (PLOTS LANGUAGE) FOR ARTWORK GENERATION TO PRODUCE PHOTOMASK SET FOR 3 x 3 ARRAY OF GTO-DEVICES; LINE 10-8020, 14 PAGES (SEE APPENDIX B AND FIGURE 3-6).

```
M2                                                          00005300
Q14 X0Y0                                                    00005310
M3                                                          00005320
Q23 X0Y0                                                    00005330
M4                                                          00005340
Q38 X0Y0                                                    00005350
M5                                                          00005360
Q40 X0Y0                                                    00005370
M7                                                          00005380
Q56 X0Y0                                                    00005390
E                                                           00005400
D05 X0Y0; D3                                                00005410
M1                                                          00005420
Q7 X0Y0                                                     00005430
M2                                                          00005440
Q15 X0Y0                                                    00005450
M3                                                          00005460
Q25 X0Y0                                                    00005470
M4                                                          00005480
Q41 X0Y0                                                    00005490
M5                                                          00005500
Q43 X0Y0                                                    00005510
M7                                                          00005520
Q57 X0Y0                                                    00005530
E                                                           00005540
D06 X0Y0; P4                                                00005550
M1                                                          00005560
Q6 X0Y0                                                     00005570
M2                                                          00005580
Q16 X0Y0                                                    00005590
M3                                                          00005600
Q26 X0Y0                                                    00005610
M4                                                          00005620
Q45 X0Y0                                                    00005630
M5                                                          00005640
Q47 X0Y0                                                    00005650
M7                                                          00005660
Q58 X0Y0                                                    00005670
E                                                           00005680
D07 X0Y0; D4                                                00005690
M1                                                          00005700
Q9 X0Y0                                                     00005710
M2                                                          00005720
Q18 X0Y0                                                    00005730
M3                                                          00005740
Q28 X0Y0                                                    00005750
M4                                                          00005760
Q49 X0Y0                                                    00005770
M5                                                          00005780
Q51 X0Y0                                                    00005790
M7                                                          00005800
Q59 X0Y0                                                    00005810
E                                                           00005820
D08 X0Y0; P1                                                00005830
Q60 X76Y76                                                  00005840
Q60 X76Y76 R2                                               00005850
Q60 X76Y76 R4                                               00005860
Q60 X76Y76 R5                                               00005870
E                                                           00005880
```

A2-10 CAD PROGRAM, PAGE 10 OF 14

A-2 COMPUTER PROGRAM (PLOTS LANGUAGE) FOR ARTWORK GENERATION TO PRODUCE PHOTOMASK SET FOR 3 x 3 ARRAY OF GTO-DEVICES; LINE 10-8020, 14 PAGES (SEE APPENDIX B AND FIGURE 3-6).

```
D69 X0Y0; D1                                                    00005890
Q61 X76Y76                                                      00005900
Q61 X76Y76 R2                                                   00005910
Q61 X76Y76 R4                                                   00005920
Q61 X76Y76R5                                                    00005930
E                                                               00005940
D70 X0Y0; P2                                                    00005950
Q62 X76Y76                                                      00005960
Q62 X76Y76 R2                                                   00005970
Q62 X76Y76 R4                                                   00005980
Q62 X76Y76 R5                                                   00005990
E                                                               00006000
D71 X0Y0; D2                                                    00006010
Q63 X76Y76                                                      00006020
Q63 X76Y76R2                                                    00006030
Q63 X76Y76 R4                                                   00006040
Q63 X76Y76 R5                                                   00006050
E                                                               00006060
D72 X0Y0; P3                                                    00006070
Q64 X76Y76                                                      00006080
Q64 X76Y76 R2                                                   00006090
Q64 X76Y76 R4                                                   00006100
Q64 X76Y76 R5                                                   00006110
E                                                               00006120
D73 X0Y0; D3                                                    00006130
Q65 X76Y76                                                      00006140
Q65 X76Y76 R2                                                   00006150
Q65 X76Y76 R4                                                   00006160
Q65 X76Y76 R5                                                   00006170
E                                                               00006180
D74 X0Y0; P4                                                    00006190
Q66 X76Y76                                                      00006200
Q66 X76Y76 R2                                                   00006210
Q66 X76Y76 R4                                                   00006220
Q66 X76Y76 R5                                                   00006230
E                                                               00006240
D75 X0Y0; D4                                                    00006250
Q67 X76Y76                                                      00006260
Q67 X76Y76 R2                                                   00006270
Q67 X76Y76 R4                                                   00006280
Q67 X76Y76 R5                                                   00006290
E                                                               00006300
Q68 X0 Y304; P1                                                 00006310
Q69 X304 Y0; D1                                                 00006320
Q70 X152 Y304;P2                                                00006330
Q71 X152 Y0; D2                                                 00006340
Q72 X304 Y304; P3                                               00006350
Q73 X0 Y0; D3                                                   00006360
Q74 X304 Y152 ;P4                                               00006370
Q75 X0 Y152; D4                                                 00006380
D101 X0Y0                                                       00006400
M1;P+ GATE 11 01                                                00006410
U X30Y70R20T20L20B20                                            00006420
W13                                                             00006430
L X0Y40.5  R80 AND 1 To7                                        00006440
L X0.5 Y40 T80 AND 1 R 67                                       00006450
U X0 Y0 R20 T20L20 B20 AND 1 R60                                00006460
W4                                                              00006470
L X0 Y10 R30                                                    00006480
```

A2-11 CAD PROGRAM, PAGE 11 OF 14

A-2 COMPUTER PROGRAM (PLOTS LANGUAGE) FOR ARTWORK GENERATION TO PRODUCE PHOTOMASK SET FOR 3 x 3 ARRAY OF GTO-DEVICES; LINE 10-8020, 14 PAGES (SEE APPENDIX B AND FIGURE 3-6).

```
W2                                                                  00006490
L X98 Y3 R13 T12 R6 T12 L24 B12 R6 B13                              00006500
M2; P+ ANODE T2 02                                                  00006510
W2.5                                                                00006520
L X101 Y6.25 R6.75 T12 R6 T5.5 L17.5 B5.5 R6 B13.25                 00006530
O X0.5 Y40.5 R79 T79 L79 B79                                        00006540
M3; N+ CATHODE T1 03                                                00006550
W13                                                                 00006560
L X15 Y61.5 R50 AND 1T37                                            00006570
L X21.5 Y55 T50 AND 1R37                                            00006580
O X100 Y40 R20 T20 L20 B20 AND 1160                                 00006590
W4                                                                  00006600
L X110 Y40 T80                                                      00006610
W2.5                                                                00006620
L X101 Y6.25 R6.75 T12 R6 T5.5 L17.5 B5.5 R6 B13.25                 00006630
M4; CONTACT OPEN (METAL REV.) 04                                    00006640
O X31 Y71 R18 T18 L18 B18                                           00006650
W11                                                                 00006660
L X16 Y61.5 R48 AND 1T37                                            00006670
L X21.5 Y56 T48 AND 1R37                                            00006680
L X1 Y46.5 R78 AND 1T67                                             00006690
L X6.5 Y41 T78 AND 1R67                                             00006700
O X0 Y0 R20 T20 L20 B20 AND 1R60                                    00006710
O X100 Y40 R20 T20 L20 B20 AND 1T60                                 00006720
W4                                                                  00006730
L X2 Y10 T24 R84 T84 R24                                            00006740
O X90Y0 R9 T15 L9 B15 AND 1R21                                      00006750
W3                                                                  00006760
L X116.5 Y12 T16.5 L27 B16.5                                        00006770
L X98 Y1.5 R14                                                      00006780
W1.5                                                                00006790
L X102 Y6.75 R5.25 T12 R6 T4.5 L10.5 B4.5 R6 B12.75                 00006800
M5;CONTACT OPEN (METAL REV.) 05                                     00006810
O X31 Y71 R18 T18 L18 B18                                           00006820
W11                                                                 00006830
L X16 Y61.5 R48 AND 1T37                                            00006840
L X21.5 Y56 T48 AND 1R37                                            00006850
L X1 Y46.5 R78 AND 1T67                                             00006860
L X6.5 Y41 T78 AND 1R67                                             00006870
O X0 Y0 R20 T20 L20 B20 AND 1R60                                    00006880
O X100 Y40 R20 T20 L20 B20 AND 1T60                                 00006890
W4                                                                  00006900
L X2 Y10 T24 R84 T84 R24                                            00006910
O X90Y0 R9 T15 L9 B15 AND 1R21                                      00006920
W3                                                                  00006930
L X116.5 Y12 T16.5 L27 B16.5                                        00006940
L X98 Y1.5 R14                                                      00006950
W1.5                                                                00006960
L X102 Y6.75 R5.25 T12 R6 T4.5 L10.5 B4.5 R6 B12.75                 00006970
M6; MESA T1 06                                                      00006980
W1                                                                  00006990
L X105 Y8.5 T13                                                     00007000
L X98.5 Y21 R13                                                     00007010
M7; CONTACT OPEN (METAL REV.) 04                                    00007011
O X31 Y71 R18 T18 L18 B18                                           00007012
W11                                                                 00007013
L X16 Y61.5 R48 AND 1T37                                            00007014
L X21.5 Y56 T48 AND 1R37                                            00007015
L X1 Y46.5 R78 AND 1T67                                             00007016
```

A2-12 CAD PROGRAM, PAGE 12 OF 14

A-2 COMPUTER PROGRAM (PLOTS LANGUAGE) FOR ARTWORK GENERATION TO PRODUCE PHOTOMASK SET FOR 3 x 3 ARRAY OF GTO-DEVICES; LINE 10-8020, 14 PAGES (SEE APPENDIX B AND FIGURE 3-6).

```
L X0.5 Y41 T78 AND 1R67                                                    00007017
U X0 Y0 R20 T20 L20 R20 AND 1R60                                           00007018
O X100 Y40 R20 T20 L20 B20 AND 1T60                                        00007019
W4                                                                         00007021
L X2 Y10 T24 R84 T84 R24                                                   00007022
O X90Y0 R9 T15 L9 B15 AND 1R21                                             00007023
W3                                                                         00007024
L X118.5 Y12 T16.5 L27 B16.5                                               00007025
L X98 Y1.5 R14                                                             00007026
W1.5                                                                       00007027
L X102 Y6.75 R5.25 T12 R6 T4.5 L16.5 B4.5 R6 B12.75                        00007028
M8; GLASS GRID ALKEY 013                                                   00007029
U X90Y0 R9 T15 L9 B15 AND 1R21                                             00007030
W3                                                                         00007040
L X116.5 Y12 T16.5 L27 B16.5                                               00007050
L X98 Y1.5 R14                                                             00007060
W1.5                                                                       00007070
L X102 Y6.75 R5.25 T12 R6 T4.5 L16.5 B4.5 R6 B12.75                        00007080
E                                                                          00007091
D102 X0Y0                                                                  00007100
M6; MESA TI 06                                                             00007110
W8                                                                         00007120
L X0 Y4 R150 T146 L146 B150                                                00007130
M8; GLASS GRID ALKEY 013                                                   00007140
W11                                                                        00007141
L X0 Y5.5 R148.5 T143 L143 B148.5                                          00007150
E                                                                          00007160
D103 X0Y0                                                                  00007170
M      6                                                                   00007180
W      8.0000 ; RING 1.0.     10.0000      0.0.     32.0000                00007190
L X    12.0000 Y    -2.1000 TO X    12.0000 Y     2.1000                  00007200
L X    12.1435 Y     1.0716 TO X    11.0565 Y     5.1284                  00007210
L X    11.4500 Y     4.1813 TO X     9.3500 Y     7.8187                  00007220
L X     9.9599 Y     6.9401 TO X     6.9401 Y     9.9599                  00007230
L X     7.8186 Y     9.3500 TO X     4.1813 Y    11.4500                  00007240
L X     5.1284 Y    11.0565 TO X     1.0716 Y    12.1435                  00007250
L X     2.1000 Y    12.0000 TO X    -2.1000 Y    12.0000                  00007260
M      8                                                                   00007270
W     11.0000 ; RING 1.0.     10.0000      0.0.     32.0000                00007280
L X    10.5300 Y    -2.1000 TO X    10.5000 Y     2.1000                  00007290
L X    10.0935 Y     0.0966 TO X     9.0565 Y     4.7534                  00007300
L X    10.1500 Y     3.4313 TO X     8.0500 Y     7.0687                  00007310
L X     8.9099 Y     5.9401 TO X     5.9401 Y     8.9099                  00007320
L X     7.0686 Y     8.0500 TO X     3.4313 Y    10.1500                  00007330
L X     4.7534 Y     9.6065 TO X     0.0966 Y    10.0935                  00007340
L X     2.1000 Y    10.5000 TO X    -2.1000 Y    10.5000                  00007350
E                                                                          00007360
D123XCY0                                                                   00007370
Q101 X16Y16                                                                00007380
Q102 X-1Y-1                                                                00007390
Q103 X137Y137                                                              00007400
Q103 X137Y15 R1                                                            00007410
Q103 X15Y15 R2                                                             00007420
Q103 X15Y137 R3                                                            00007430
E                                                                          00007440
D105 X0Y0                                                                  00007450
M6; MESA TI 06                                                             00007460
W8                                                                         00007470
L X0 Y4 R150 T146 L146 B150                                                00007480
```

A2-13 CAD PROGRAM, PAGE 13 OF 14

A-2 COMPUTER PROGRAM (PLOTS LANGUAGE) FOR ARTWORK GENERATION TO PRODUCE PHOTOMASK SET FOR 3 x 3 ARRAY OF GTO-DEVICES; LINE 10-8020, 14 PAGES (SEE APPENDIX B AND FIGURE 3-6).

```
M8; GLASS GRID 012                                                                                                00007490
W11                                                                                                               00007500
L X0 Y5.5 R148.5 T143 L143 B148.5                                                                                 00007510
E                                                                                                                 00007520
D104 X0Y0                                                                                                         00007530
M     6                                                                                                           00007540
W      8.0000 ; RING I.D.      10.0000      O.D.      32.0000                                                      00007550
L X    12.0000 Y    -2.1000 TU X    12.0000 Y     2.1000                                                         00007560
L X    12.1435 Y     1.0716 TU X    11.0565 Y     5.1284                                                         00007570
L X    11.4500 Y     4.1813 TU X     9.3500 Y     7.8187                                                         00007580
L X     9.9599 Y     6.9901 TU X     6.9901 Y     9.9599                                                         00007590
L X     7.8186 Y     9.3500 TU X     4.1813 Y    11.4500                                                         00007600
L X     5.1284 Y    11.0565 TU X     1.0716 Y    12.1435                                                         00007610
L X     2.1000 Y    12.0000 TU X    -2.1000 Y    12.0000                                                         00007620
M     6                                                                                                           00007630
W     -11.0000 ; RING I.D.      10.0000      O.D.      32.0000                                                     00007640
L X    10.5000 Y    -2.1000 TU X    10.5000 Y     2.1000                                                         00007650
L X    10.0935 Y     0.6966 TU X     9.6065 Y     4.7534                                                         00007660
L X    10.1500 Y     3.4313 TU X     8.0500 Y     7.0687                                                         00007670
L X     8.9099 Y     5.9401 TU X     5.9401 Y     8.9099                                                         00007680
L X     7.0686 Y     8.0500 TU X     3.4313 Y    10.1500                                                         00007690
L X     4.7534 Y     9.6065 TU X     0.6966 Y    10.0935                                                         00007700
L X     2.1000 Y    10.5000 TU X    -2.1000 Y    10.5000                                                         00007710
E                                                                                                                 00007711
D106X0Y0                                                                                                          00007720
Q105 X-1Y-1                                                                                                       00007730
Q104 X137Y137                                                                                                     00007740
Q104 X137Y15 R1                                                                                                   00007750
Q104 X15Y15 R2                                                                                                    00007760
Q104 X15Y137 R3                                                                                                   00007770
E                                                                                                                 00007780
Q123 X152 Y152                                                                                                    00007790
Q106 X0 Y304 ANU 2R152                                                                                            00007800
Q106 X0 Y152 ANU 1R304                                                                                            00007810
Q106 X0 Y0 ANU 2R152                                                                                              00007820
D76 XCY0; OUTBURDER                                                                                               00007830
W8                                                                                                                00007840
L X-10Y-6 R472 T468 L468 B472                                                                                     00007850
E                                                                                                                 00007860
M1                                                                                                                00007870
Q76 X0Y0                                                                                                          00007880
M2                                                                                                                00007890
Q76 X0Y0                                                                                                          00007900
M3                                                                                                                00007910
Q76 X0Y0                                                                                                          00007920
M4                                                                                                                00007930
Q76 X0Y0                                                                                                          00007940
M5                                                                                                                00007950
Q76 X0Y0                                                                                                          00007960
M6                                                                                                                00007970
Q76 X0Y0                                                                                                          00007980
M7                                                                                                                00007990
Q76 X0Y0                                                                                                          00008000
M8                                                                                                                00008010
Q76 X0Y0                                                                                                          00008020
```

A2-14 CAD PROGRAM, PAGE 14 OF 14

A-2 COMPUTER PROGRAM (PLOTS LANGUAGE) FOR ARTWORK GENERATION TO PRODUCE PHOTOMASK SET FOR 3 x 3 ARRAY OF GTO-DEVICES; LINE 10-8020, 14 PAGES (SEE APPENDIX B AND FIGURE 3-6).

APPENDIX B

PHOTO MASK SET FOR 3x3 ARRAY OF GTO DEVICES

The mask set for fabrication of the test geometries used for studying the behavior of GTO devices is shown in this appendix Figure B-1a to B-1f.

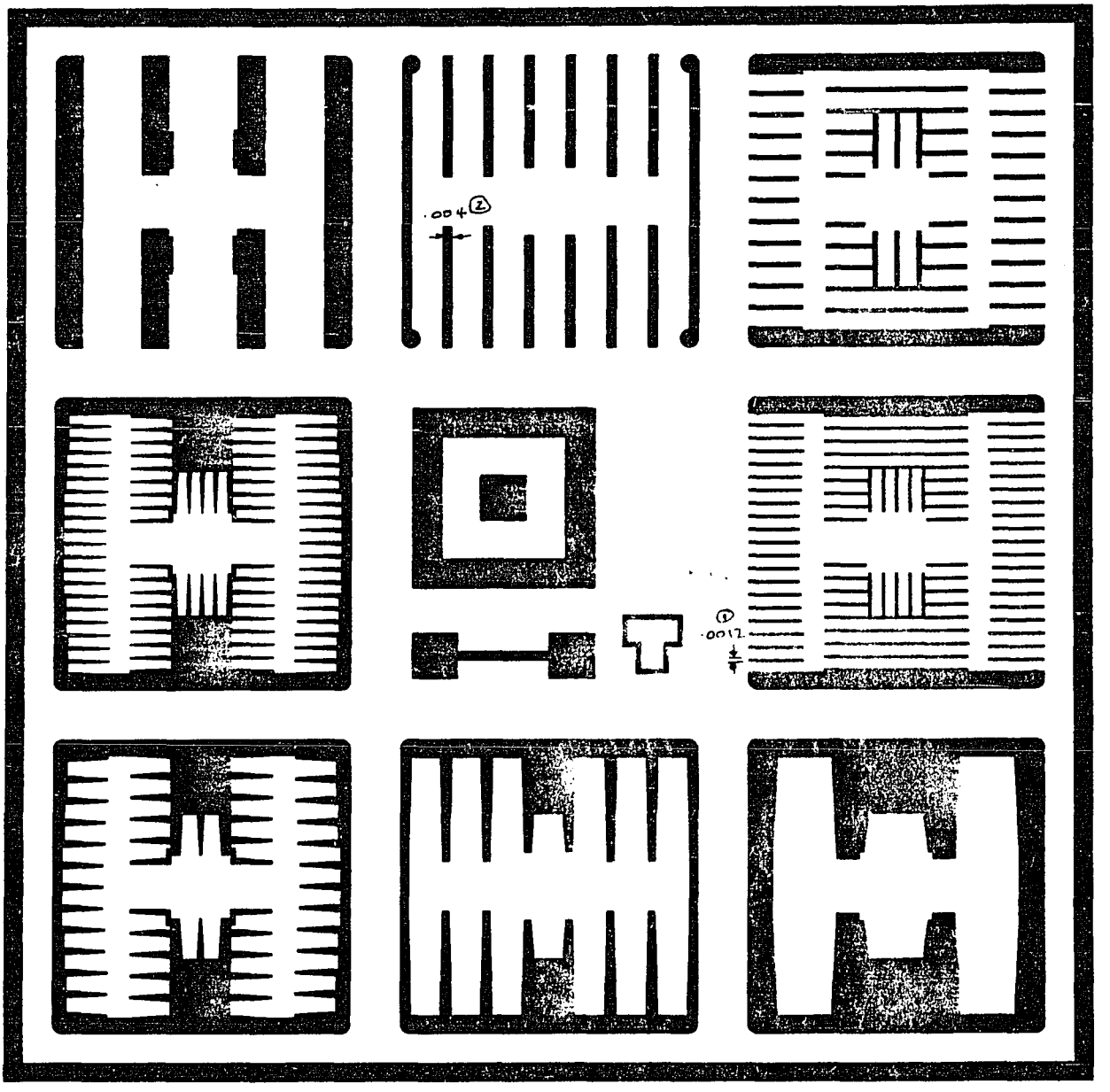


FIGURE B-1a MO1, P^+ GATE CONTACT DIFFUSION

FIGURE B-1 PHOTOMASK SET FOR FABRICATION OF 3 X 3 ARRAY OF GTO TEST GEOMETRIES, CENTER CONTAINS DIAGNOSTICS AND ALIGNMENT PATTERN. (FOR DIMENSIONS AND USE IN PROCESS SEE PP 53-55, AND 56-58, RESPECTIVELY)

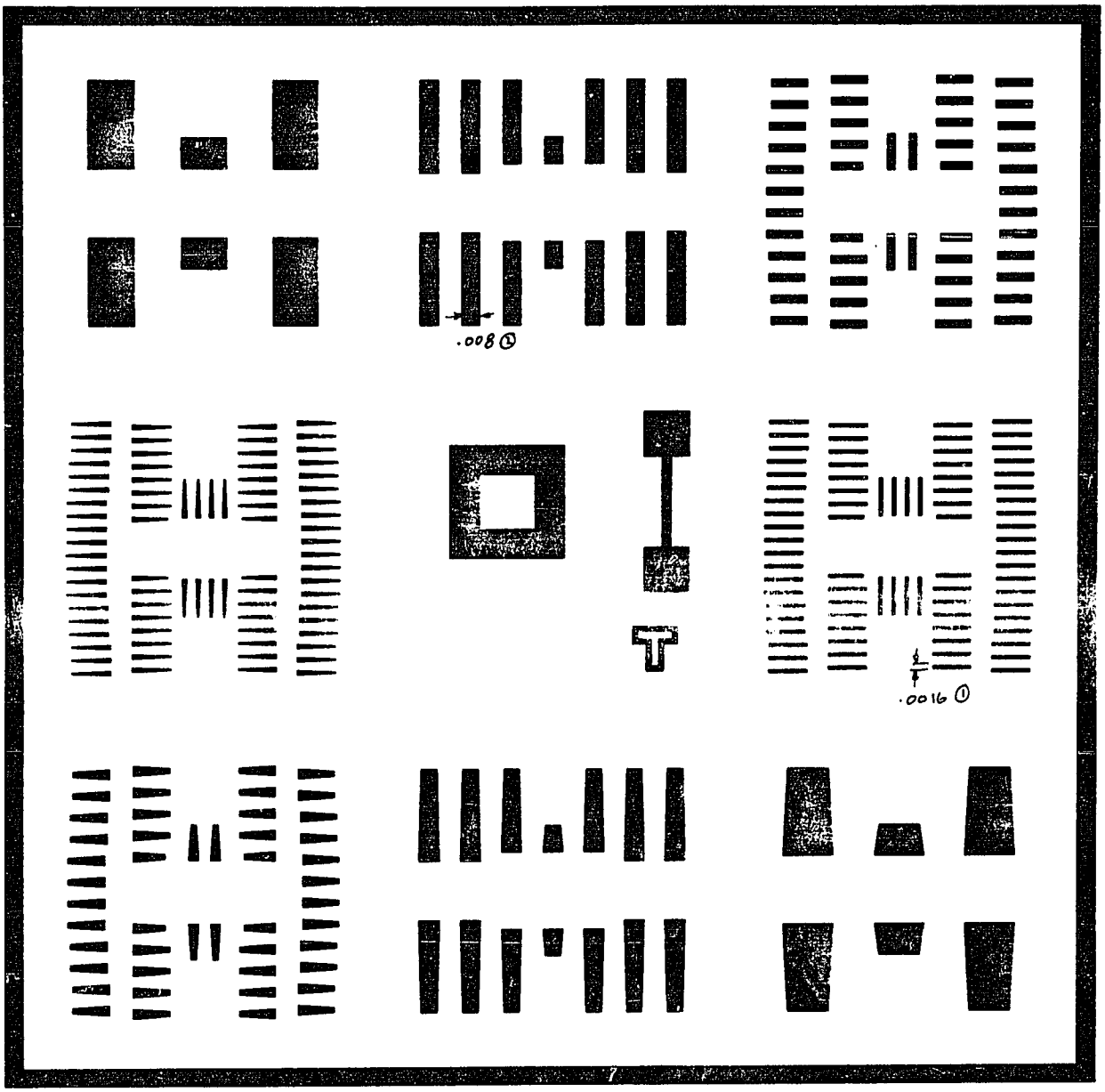


FIGURE B-1b MO3, CATHODE EMITTER DIFFUSION

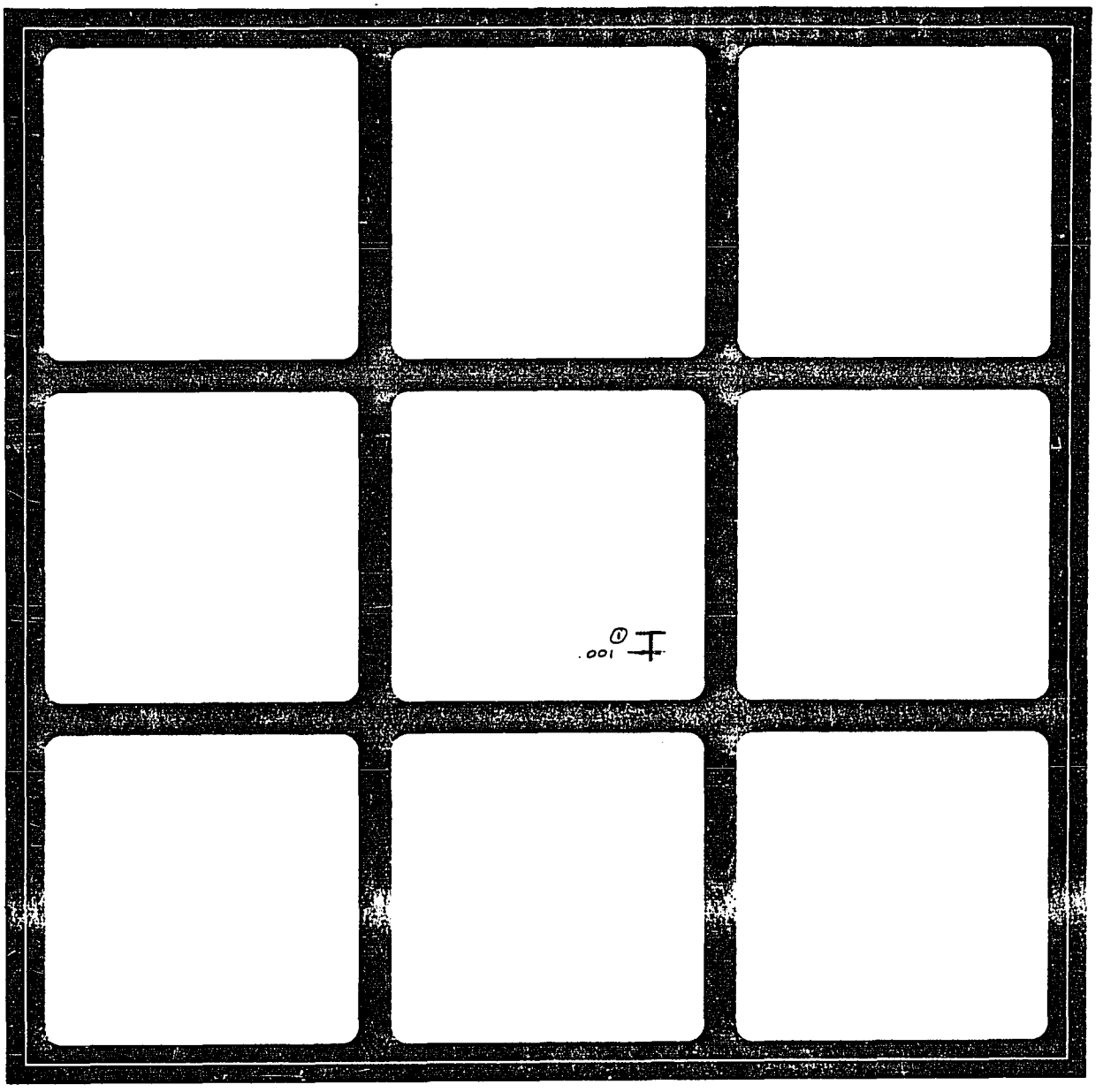


FIGURE B-1c M06, MESA DEFINITION

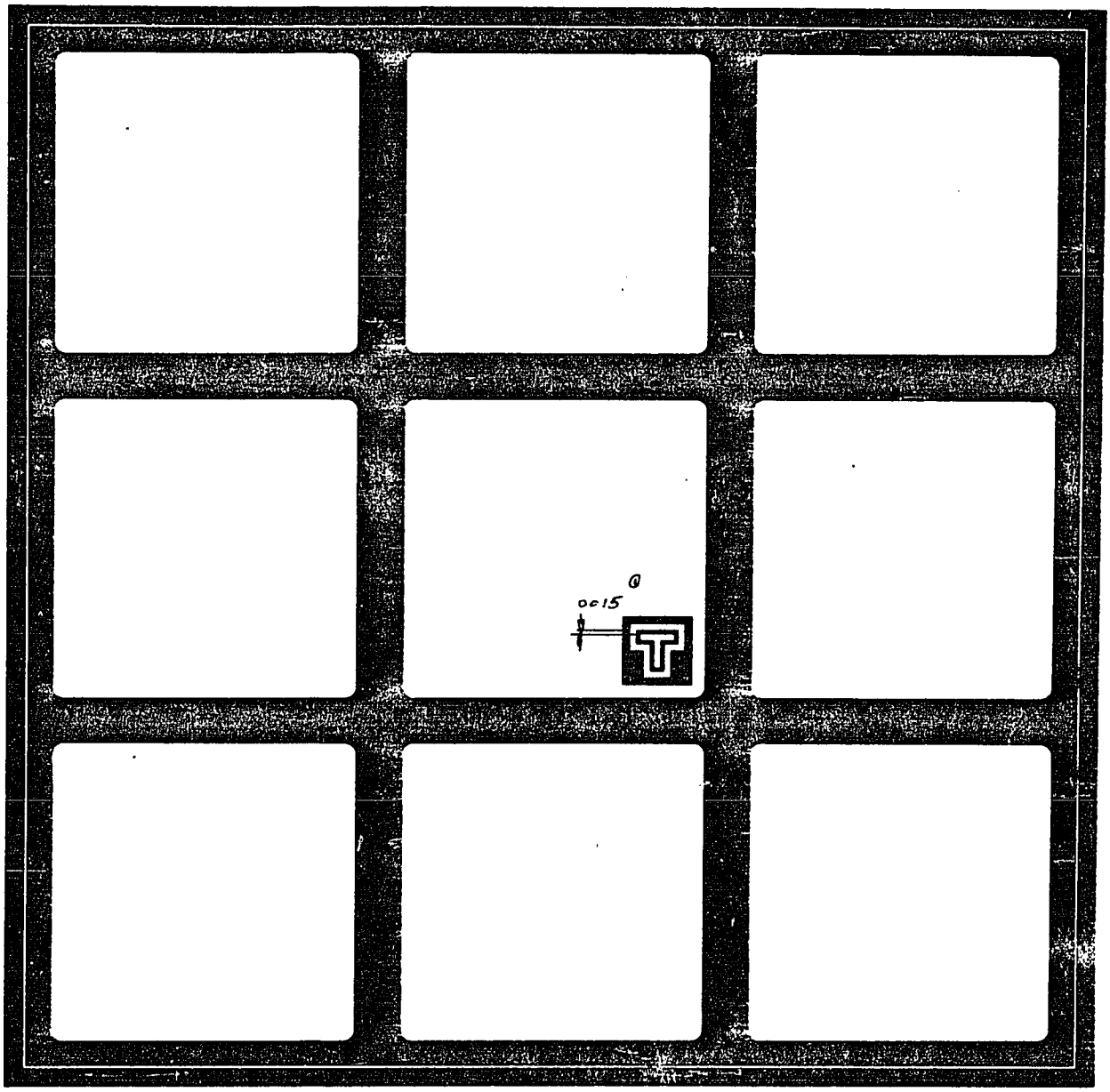


FIGURE B-1d MO8, OXIDE SHELF REMOVAL

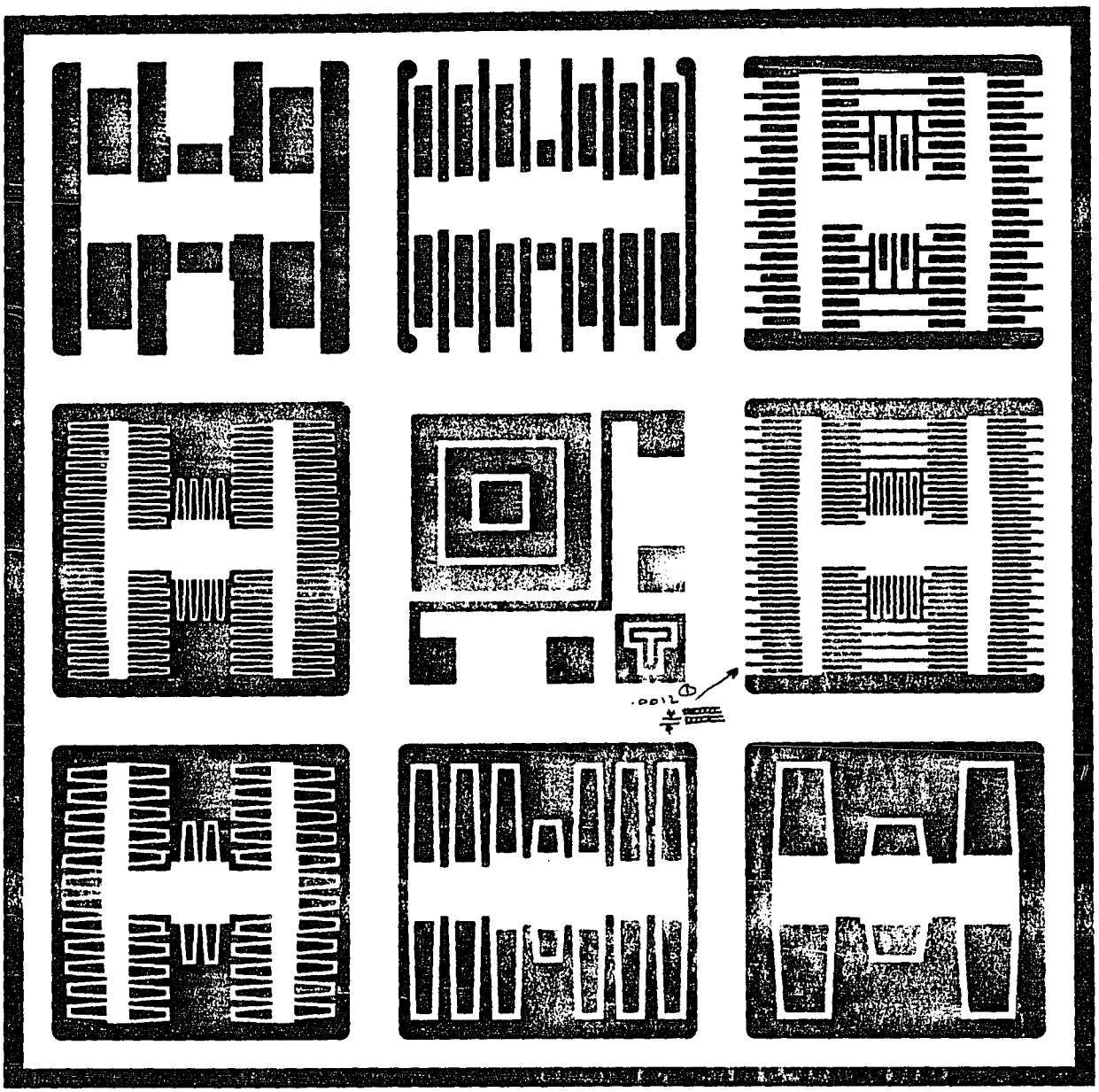


FIGURE B-1e MO4, GATE AND CATHODE CONTACT OPEN

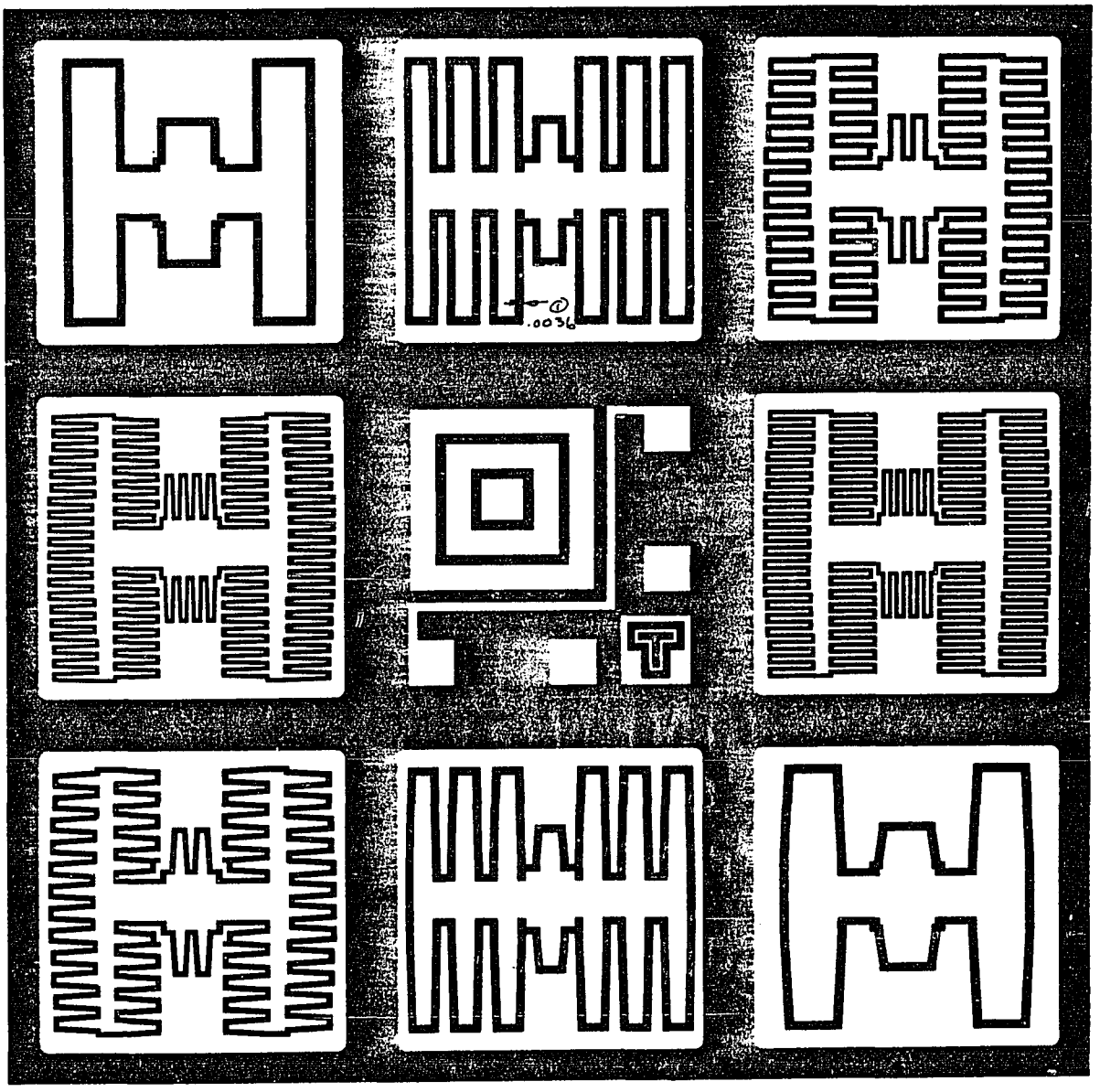


FIGURE B-1f MO7, DEFINE METAL ELECTRODES

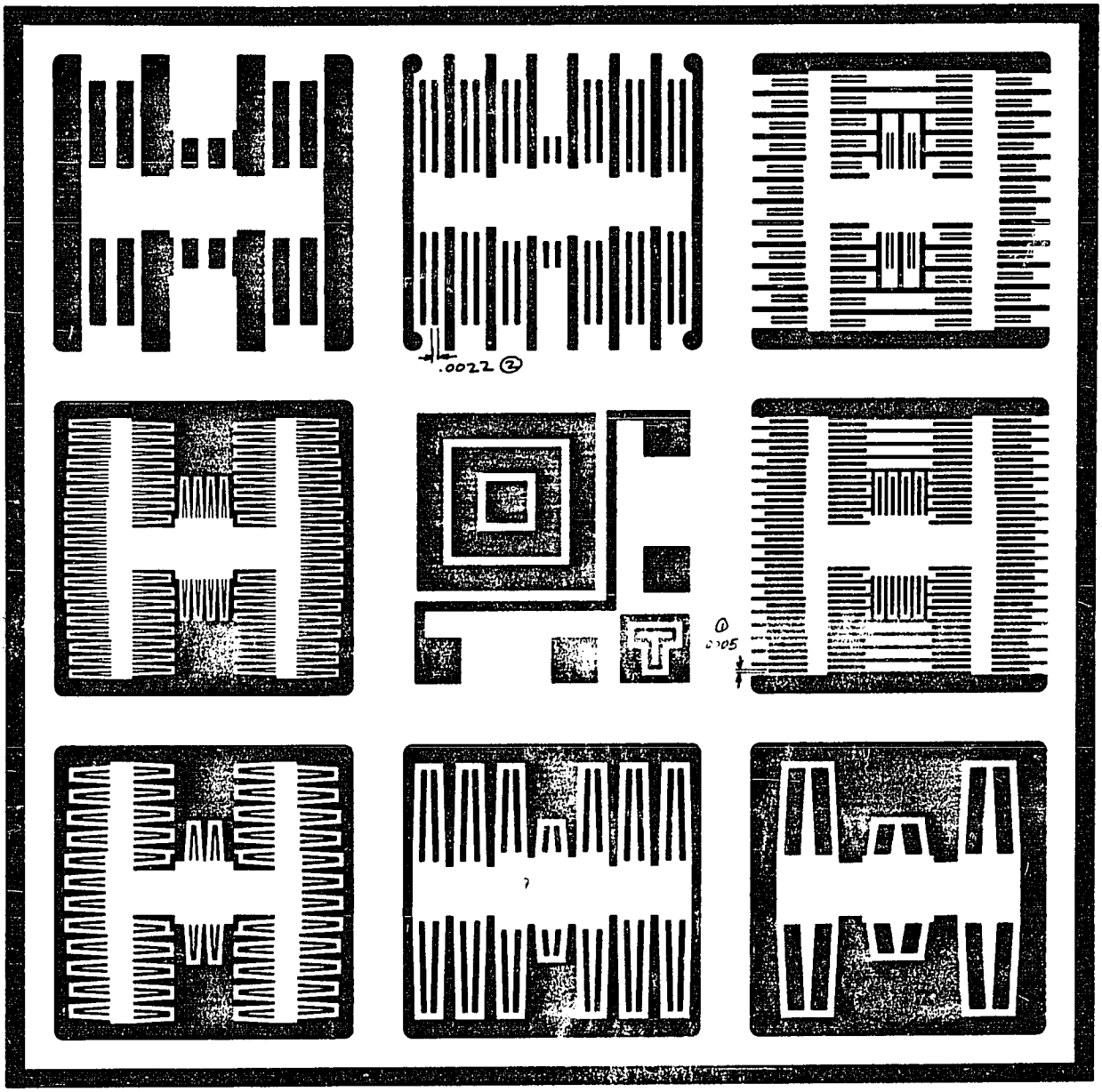


FIGURE B-1g MO5, GATE AND CATHODE CONTACT OPEN (DEFOCUS)

APPENDIX C

STATIC DATA FOR GTO'S WITH STANDARD CATHODE AND DYNAMICALLY BALLASTED CATHODE

A printout of static data from computer tested gate turn-off thyristors is given in this appendix.

Figure C-1 shows the data for GTO's of Device Type 3 with an all-epitaxial structure and a standard 0.7Ω/square cathode diffusion (series 97E).

Figure C-2 shows the data for GTO's of Device Type 3 having a 20Ω/square resistively ballasted, defocused cathode (series 97H).

The first line in these data tables gives the quantity measured, current or voltage. The second line specifies the voltage or current at which the value for this measured parameter is recorded, except for I_{gt}, where it is the maximum trigger current available. The third line indicates the upper limit of the computer range. R_{GK} is a resistor added in parallel to the gate-cathode.

LOT 97-E 11/16/78

TESTED TO

G4000-5 H. BECKE 11/3/77

UNIT	VDRXM 10.0UA 700V RGK=1K V	VDRXM 200.UA 700V RGK=1K V	IDRXM 500V 1000UA RGK=1K UA	IDRXM 450V 1000UA RGK=1K UA	IDRXM 250V 1000UA RGK=1K UA	IDRXM 225V 1000UA RGK=1K UA	IDRXM 125V 1000UA RGK=1K UA	IDRXM 115V 1000UA RGK=1K UA	IDRXM 20V 10.0UA RGK=1K UA	VKA .500MA 100 V V
1	716.	716.	1.	1.	.	1.	.	.	.05	93.2
2	7.	716.	20.	20.	19.	19.	19.	19.	10.23	95.8
3	672.	678.	.	.	.	.	.	.	-.19	87.5
4	716.	716.	.	.	.	.	.	.	-.17	92.8
5	144.	172.	1023.	1023.	1023.	1023.	1.	.	-.12	91.3
6	716.	716.	.	.	.	.	.	.	-.13	94.8
7	4.	716.	16.	16.	15.	15.	15.	15.	10.23	96.4
8	716.	716.	2.	2.	2.	2.	2.	2.	1.81	98.9
9	716.	716.	2.	2.	1.	2.	1.	1.	1.06	95.7
10	13.	716.	10.	10.	10.	10.	10.	10.	9.43	95.4
11	679.	690.	.	.	.	.	.	.	-.16	99.0
12	8.	716.	14.	14.	14.	13.	13.	13.	10.23	85.8
13	285.	366.	1023.	1023.	7.	5.	4.	4.	3.41	98.9
14	698.	705.	.	.	.	.	.	.	-.12	84.7
15	654.	676.	2.	2.	1.	1.	2.	1.	1.00	93.5
16	716.	716.	.	.	.	.	.	.	-.13	92.7
17	716.	716.	.	.	.	.	.	.	-.17	81.0
18	716.	716.	4.	4.	4.	4.	4.	4.	3.67	95.5
19	716.	716.	1.	1.	1.	1.	1.	1.	.78	95.8
20	716.	716.	1.	.	.	.	.	.	-.11	97.2
21	17.	716.	10.	10.	10.	10.	9.	9.	8.67	73.8
22	108.	134.	1023.	1023.	1023.	1023.	92.	39.	-.12	96.3
23	716.	716.	7.	7.	7.	7.	7.	7.	6.32	98.9
24	716.	716.	.	.	.	.	.	.	-.12	96.7
25	654.	666.	.	.	.	.	.	.	-.16	91.6
26	716.	716.	.	.	-1.	.	.	.	-.15	55.6
27	716.	716.	.	.	.	.	.	.	-.16	89.1
28	716.	716.	2.	2.	2.	2.	2.	2.	1.79	94.1
29	716.	716.	.	.	.	1.	1.	1.	.03	89.0

FIGURE C-1a FORWARD BLOCKING V_{DRXM}, REVERSE LEAKAGE I_{DRXM}, REVERSE BLOCKING V_{KA}

FIGURE C-1 STATIC DATA OF COMPUTER-TESTED ALL-EPITAXIAL GTO-THYRISTORS. LOT 97E; STANDARD CATHODE, $R_{SK} \sim 0.7\,\Omega/\square$ (SEE CHAPTER IV, TABLE 4-1)

LOT 97-E 11/16/78

TESTED TO

G4000-5 H. BECKE 11/3/77

	IGT1+ 30 100UA	IGT1+ 30 1000UA	IGT1+ 30 10MA	IGT1+ 30 100MA	VGT1+ 30 10V	VKG .500MA 100 V	VT1 1A 10MA	VT1 5A 10MA	VT1 10A 10MA	VT1 15A 10MA
UNIT	UA	UA	MA	MA	V	V	V	V	V	V
1	77.6	87.	.20	1.6	.66	17.2	.85	1.02	1.18	1.31
2	57.4	67.	.14	1.5	.62	17.0	.87	1.01	1.17	1.30
3	94.4	102.	.20	1.6	.61	17.7	.87	1.04	1.18	1.32
4	87.7	96.	.20	1.6	.64	17.7	.87	1.03	1.17	1.30
5	99.3	108.	.21	1.7	.56	17.3	.87	1.02	1.17	1.31
6	102.3	117.	.21	1.7	.63	17.5	.87	1.02	1.18	1.32
7	44.6	53.	.13	1.4	.68	17.1	.87	1.04	1.17	1.30
8	65.6	74.	.18	1.5	.64	17.4	.86	1.02	1.17	1.30
9	63.5	72.	.19	1.5	.55	17.1	.86	1.03	1.16	1.29
10	60.8	70.	.16	1.5	.63	17.1	.86	1.02	1.17	1.30
11	89.0	97.	.20	1.6	.63	17.6	.86	1.03	1.17	1.31
12	65.2	75.	.16	1.5	.64	17.1	.86	1.03	1.18	1.31
13	60.6	69.	.18	1.5	.60	17.1	.86	1.01	1.17	1.30
14	95.0	103.	.21	1.6	.63	17.5	.86	1.02	1.17	1.30
15	60.4	69.	.18	1.5	.60	17.5	.86	1.01	1.17	1.31
16	89.0	97.	.21	1.6	.56	16.8	.85	1.01	1.17	1.30
17	66.0	74.	.19	1.5	.63	17.8	.85	1.02	1.16	1.30
18	63.5	72.	.18	1.5	.61	17.1	.87	1.03	1.17	1.30
19	62.0	71	.19	1.5	.66	17.1	.87	1.04	1.17	1.29
20	68.0	77.	.19	1.5	.64	17.6	.86	1.02	1.17	1.30
21	73.6	83.	.17	1.5	.64	17.0	.87	1.03	1.17	1.31
22	85.5	93.	.20	1.6	.66	17.7	.86	1.03	1.17	1.30
23	52.9	62.	.16	1.5	.55	17.2	.87	1.04	1.17	1.31
24	92.7	101.	.20	1.6	.63	17.8	.86	1.02	1.17	1.30
25	93.8	102.	.21	1.6	.63	17.4	.86	1.02	1.17	1.30
26	91.1	100.	.21	1.6	.63	17.4	.86	1.02	1.18	1.31
27	68.3	77.	.19	1.6	.57	17.9	.86	1.02	1.16	1.30
28	55.9	65.	.18	1.5	.68	17.5	.86	1.02	1.17	1.30
29	66.2	75.	.19	1.6	.62	17.5	.86	1.02	1.17	1.30

FIGURE C-1b GATE TRIGGER CURRENT I_{gt}
ON STATE VOLTAGE $V_T = f(I_T)$

LOT 97-E 11/16/78

TESTED TO

G4000-5 H. BECKE 11/3/77

UNIT	VT1 30A 10MA V	VT1 50A 10MA V	VT1 70A 10MA V	VT1 1A 100MA V	VT1 5A 100MA V	VT1 10A 100MA V	VT1 15A 100MA V	VT1 30A 100MA V	VT1 50A 100MA V	VT1 70A 100MA V
1	1.70	2.19	2.74	.87	1.04	1.18	1.31	1.70	2.20	2.74
2	1.68	2.16	2.69	.88	1.04	1.17	1.30	1.68	2.16	2.69
3	1.73	2.24	2.82	.87	1.04	1.18	1.32	1.73	2.25	2.82
4	1.69	2.18	2.72	.87	1.02	1.17	1.30	1.69	2.19	2.73
5	1.69	2.18	2.71	.86	1.03	1.17	1.30	1.69	2.18	2.71
6	1.72	2.22	2.78	.86	1.03	1.18	1.32	1.72	2.22	2.78
7	1.68	2.15	2.68	.86	1.01	1.17	1.30	1.68	2.15	2.68
8	1.69	2.18	2.71	.86	1.02	1.17	1.30	1.69	2.18	2.71
9	1.67	2.14	2.66	.86	1.01	1.16	1.29	1.67	2.14	2.66
10	1.67	2.15	2.66	.86	1.01	1.17	1.30	1.67	2.15	2.67
11	1.69	2.19	2.73	.86	1.01	1.17	1.31	1.69	2.19	2.73
12	1.70	2.19	2.73	.86	1.03	1.18	1.31	1.70	2.19	2.73
13	1.68	2.16	2.68	.86	1.03	1.17	1.30	1.68	2.16	2.69
14	1.68	2.16	2.69	.86	1.03	1.17	1.30	1.68	2.16	2.69
15	1.70	2.19	2.74	.86	1.03	1.17	1.31	1.70	2.19	2.74
16	1.69	2.18	2.71	.87	1.02	1.17	1.30	1.69	2.18	2.71
17	1.68	2.16	2.70	.87	1.02	1.16	1.30	1.68	2.16	2.70
18	1.68	2.16	2.69	.87	1.02	1.17	1.30	1.68	2.16	2.69
19	1.67	2.14	2.66	.87	1.02	1.16	1.29	1.67	2.14	2.66
20	1.69	2.17	2.71	.86	1.02	1.17	1.30	1.68	2.17	2.71
21	1.69	2.18	2.71	.87	1.02	1.17	1.31	1.69	2.18	2.71
22	1.69	2.18	2.71	.86	1.01	1.17	1.30	1.69	2.18	2.71
23	1.70	2.19	2.74	.86	1.01	1.17	1.31	1.70	2.19	2.74
24	1.68	2.17	2.70	.86	1.01	1.17	1.30	1.68	2.17	2.70
25	1.69	2.18	2.71	.86	1.01	1.17	1.30	1.69	2.18	2.71
26	1.70	2.20	2.74	.86	1.03	1.17	1.31	1.70	2.20	2.74
27	1.68	2.16	2.70	.86	1.01	1.16	1.30	1.68	2.16	2.70
28	1.68	2.16	2.69	.86	1.03	1.17	1.30	1.68	2.16	2.69
29	1.68	2.17	2.70	.86	1.01	1.17	1.30	1.68	2.17	2.70

FIGURE C-1c ON-STATE VOLTAGE $V_T = f(I_T)$

G-4000-5 LOT#97H H. BECKE 11/30/78

TESTED TO

G4000-5 H. BECKE 11/3/77

UNIT	VDRXM 10.0UA 700V RGK=1K V	VDRXM 200.UA 700V RGK=1K V	IDRXM 500V 1000UA RGK=1K UA	IDRXM 450V 1000UA RGK=1K UA	IDRXM 250V 1000UA RGK=1K UA	IDRXM 225V 1000UA RGK=1K UA	IDRXM 125V 1000UA RGK=1K UA	IDRXM 115V 1000UA RGK=1K UA	IDRXM 20V 10.0UA RGK=1K UA	VKA .500MA 100 V V
1	288.	507.	211.	129.	4.	2.	.	.	-.12	97.6
2	411.	716.	26.	16.	1.	1.	.	.	-.20	95.7
3	381.	716.	11.	10.	8.	8	7.	7.	4.85	56.8
4	716.	716.	2.	1.	1.	1.	1.	1.	.03	85.6
5	696.	716.	1.	1.	.	.	.	.	-.09	86.9
6	591.	716.	4.	2.	.	.	.	.	-.18	55.2
7	476	716.	15.	8.	.	.	.	.	-.10	84.9
8	109.	380.	1023.	464.	53.	37.	10.	9.	7.24	52.3
9	716.	716.	1.	1.	1	1.	1.	1.	-.05	99.0
10	642.	716.	8.	7.	6.	6.	5.	5.	3.79	66.6
11	716.	716.	2.	1.	1.	1.	1.	.	-.01	94 7
12	530.	716.	8.	6.	2.	2.	2.	2.	1.15	93.7
13	81.	211.	1023.	1023.	473.	297.	23.	18.	5.57	95.7
14	520.	716.	9.	5.	.	.	.	.	-.08	99.0
15	261.	537.	167.	115.	9.	5.	.	.	-.13	94.1
16	716.	716.	3.	3.	2.	2.	1.	1.	.26	97.1
17	716.	716.	1.	1.	1.	1.	1.	1.	-.03	98.1
18	604.	716.	3.	2.	.	.	.	.	-.14	68.1
19	324.	683.	57.	40.	3.	2.	.	.	-.20	99.0
20	333.	598.	98.	61.	2.	1.	.	.	-.10	93.0
21	469.	716.	17.	9.	.	.	.	.	-.20	81.3
22	643.	716.	2.	1.	.	.	.	.	-.16	98.9
23	6.	716.	21	18.	13.	13.	13.	13.	10.23	90.7
24	716.	716.	1.	1.	1.	1.	1	1.	-.05	96.9

FIGURE C-2a FORWARD BLOCKING V_{DRXM}, REVERSE LEAKAGE I_{DRXM}, REVERSE BLOCKING V_{KA}

FIGURE C-2 STATIC DATA OF COMPUTER-TESTED ALL-EPITAXIAL GTO-THYRISTORS. LOT 97H; IMPLANTED, DEFOCUSED CATHODE, $R_{SK} \sim 20\ \Omega/\square$

G-4000-5 LOT#97H H. BECKE 11/30/78

TESTED TO

G4000-5 H. BECKE 11/3/77

UNIT	IGT1+ 30 100UA UA	IGT1+ 30 1000UA UA	IGT1+ 30 10MA MA	IGT1+ 30 100MA MA	VGT1+ 30 10V V	VKG .500MA 100 V V	VT1 1A 10MA V	VT1 5A 10MA V	VT1 10A 10MA V	VT1 15A 10MA V
1	102.3	255.	.32	1.8	.72	19.0	.99	1.30	1.52	1.71
2	102.3	303.	.37	1.8	.72	19.2	.99	1.30	1.51	1.70
3	102.3	483.	.56	1.8	.75	19.8	1.05	1.38	1.61	1.82
4	102.3	500.	.57	1.8	.71	14.6	1.02	1.34	1.56	1.76
5	102.3	276.	.34	1.8	.72	17.9	.98	1.30	1.52	1.72
6	102.3	281.	.35	1.8	.71	19.4	.98	1.30	1.52	1.71
7	102.3	230.	.30	1.8	.72	6.8	1.00	1.29	1.52	1.72
8	102.3	509.	.57	1.8	.65	19.8	1.02	1.33	1.56	1.76
9	102.3	331.	.40	1.8	.72	20.0	1.00	1.30	1.53	1.73
10	102.3	459.	.53	1.8	.75	19.9	1.06	1.39	1.62	1.82
11	102.3	451.	.52	1.8	.75	19.9	1.02	1.34	1.58	1.77
12	102.3	275.	.34	1.8	.64	20.0	1.00	1.28	1.50	1.69
13	102.3	306.	.36	1.7	.64	20.1	1.00	1.31	1.55	1.75
14	102.3	348.	.42	1.8	.73	20.0	1.01	1.32	1.54	1.74
15	102.3	363.	.43	1.8	.75	17.2	1.01	1.30	1.55	1.75
16	102.3	256.	.32	1.6	.72	19.1	1.00	1.30	1.52	1.72
17	102.3	304.	.37	1.8	.64	20.0	.99	1.27	1.53	1.73
18	102.3	291.	.36	1.8	.67	14.5	.99	1.28	1.51	1.71
19	102.3	321.	.39	1.8	.71	20.0	1.01	1.29	1.53	1.73
20	102.3	237.	.30	1.7	.72	20.1	1.01	1.30	1.54	1.73
21	102.3	234.	.29	1.7	.64	13.5	.99	1.29	1.51	1.71
22	102.3	247.	.31	1.7	.72	19.8	1.01	1.30	1.54	1.74
23	102.3	390.	.45	1.8	.74	20.0	1.01	1.33	1.54	1.74
24	101.3	335	40	1.8	.71	19.9	1.01	1.30	1.55	1.75

FIGURE C-2b GATE TRIGGER CURRENT I_{gt}, ON-STATE VOLTAGE $V_T = f(I_T)$

G-4800-5 LOT#97H H. BECKE 11/30/78

TESTED TO

G4800-5 H. BECKE 11/3/77

UNIT	VT1 30A 10MA V	VT1 50A 10MA V	VT1 70A 10MA V	VT1 1A 100MA V	VT1 5A 100MA V	VT1 10A 100MA V	VT1 15A 100MA V	VT1 30A 100MA V	VT1 50A 100MA V	VT1 70A 100MA V
1	2.23	2.83	3.49	.99	1.28	1.52	1.71	2.23	2.83	3.50
2	2.20	2.79	3.43	.99	1.29	1.51	1.70	2.20	2.79	3.43
3	2.35	2.98	3.67	1.05	1.37	1.61	1.82	2.35	2.98	3.66
4	2.29	2.91	3.60	1.04	1.33	1.56	1.76	2.29	2.91	3.60
5	2.24	2.86	3.53	.99	1.27	1.52	1.72	2.24	2.86	3.53
6	2.23	2.83	3.48	.99	1.29	1.52	1.71	2.23	2.83	3.48
7	2.23	2.83	3.47	.99	1.30	1.52	1.72	2.23	2.83	3.47
8	2.28	2.91	3.59	1.02	1.31	1.56	1.76	2.28	2.91	3.59
9	2.25	2.86	3.53	1.00	1.30	1.54	1.73	2.25	2.87	3.53
10	2.36	2.99	3.67	1.06	1.38	1.62	1.82	2.36	2.99	3.67
11	2.31	2.93	3.61	1.02	1.33	1.58	1.78	2.30	2.93	3.61
12	2.20	2.79	3.43	1.00	1.28	1.50	1.69	2.20	2.79	3.43
13	2.28	2.91	3.59	1.00	1.31	1.55	1.75	2.28	2.91	3.60
14	2.25	2.86	3.51	1.00	1.31	1.54	1.74	2.25	2.86	3.51
15	2.27	2.88	3.55	1.01	1.30	1.55	1.75	2.27	2.88	3.55
16	2.24	2.84	3.50	1.00	1.30	1.53	1.72	2.24	2.85	3.51
17	2.25	2.88	3.57	1.01	1.30	1.53	1.73	2.25	2.88	3.57
18	2.22	2.82	3.47	1.01	1.28	1.52	1.71	2.22	2.82	3.47
19	2.25	2.87	3.54	1.01	1.32	1.53	1.73	2.25	2.87	3.54
20	2.25	2.86	3.51	1.01	1.30	1.54	1.73	2.25	2.86	3.52
21	2.21	2.81	3.45	1.00	1.29	1.51	1.71	2.21	2.81	3.45
22	2.26	2.87	3.53	1.01	1.30	1.54	1.74	2.26	2.87	3.53
23	2.25	2.86	3.52	1.01	1.32	1.54	1.74	2.25	2.86	3.52
24	2.28	2.90	3.58	1.01	1.32	1.55	1.75	2.28	2.90	3.58

FIGURE C-2c ON STATE VOLTAGE $V_T = f(I_T)$

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ATTACHMENT

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