RELIABILITY OF MOS DEVICES - THRESHOLD VOLTAGE INSTABILITY

BY

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<u>VITA</u>

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ABSTRACT

A very important factor in the reliability of
MOS devices is the stability of the threshold voltage.
This dissertation examines the effects of positive and
negative gate bias stresses at elevated temperatures
on the drift in the threshold voltage of MOS field effect
transistors.

Over 400 p-channel enhancement mode devices were
life tested under different temperature and gate bias
conditions for periods of up to 15,000 hours, and
the drift in their threshold voltages studied and
analyzed. It was found that under both negative and
positive bias-temperature tests, the threshold voltage
drifted towards more negative values, though in the
negative bias tests, the drift in the first few tens
or hundreds of hours was in the opposite direction.

The effect of positive bias is easily explained in
terms of impurity ion migration effects. To explain the
effect of negative bias, two competing mechanisms,
namely, impurity ion migration and the silicon ion
effects, are postulated by the author; and a logical
theoretical explanation is developed to explain the
results of the experimental investigation.

APPROVAL OF DISSERTATION

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For

Department of Electrical Engineering
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By

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CHAPTER 1

I N T R O D U C T I O N

1.1 Historical Review:

An unipolar field-effect transistor was described by Shockley in 1952[1]. Such transistors were built, tested, and their performance analyzed by Dacey and Ross[2]. However, the device was only in the laboratory stage of development, until advances in semiconductor technology made its fabrication in the industry feasible[3,4].

The insulated gate construction was developed and described by Hofstein, Heiman and others[5,6]. The high input impedance and fast switching speeds of these devices made the insulated-gate field-effect transistor a complement to the bipolar transistor for many applications, and helped in the complete transistorization of the older electron tube circuits.

This revival of interest in the field-effect transistor (FET) in the early sixties led Wallmark[7] to hail its advent as an "Old Device with New Promise". The theory and performance of the FET have since been studied and formulated in great depth.[8,9,10]. Later, Sah and Pao[11] presented a detailed theory,

summarizing the results of all previous investigations on the Metal-Oxide-Semiconductor (MOS) FET. (See also 12 and 13). The further development of MOS technology led to its easy adoption in the design and fabrication of the present day integrated circuits.[14,15,16]

1.2 Oxidation:

The gate oxide is an important part of the MOS structure. The oxidation of silicon is usually accomplished by thermal growth, which has been described in detail by Seely and others.[17,18] Oxidation at lower temperatures using Si_3N_4 masks have been reported on.[19] Oxides have also been prepared by chemical vapor deposition using $SiH_4-CO_2-H_2$ sources and have been compared with thermally grown oxides by Gaind and others.[20]

The impurities in thermally grown oxide layers have been analyzed using electron microprobe techniques.[21] Defects such as pinholes in thermal oxides have been studied[22]. Deal[23] has presented a concise summary of the nature and properties of all the charges found in thermally grown oxides.

1.3 The Silicon - Silicon Dioxide System:

The characteristics and operation of a MOS

device depend heavily on the properties of the

silicon - silicon dioxide interface. A consider-

able amount of study over the years has been devoted

to the properties of the silicon - silicon dioxide

system and to correlate them to the observed

electrical characteristics of MOS devices.[24] These

studies have established the existence of the

following:

a) Fast surface states at the silicon-silicon dioxide interface.

b) Fixed positive surface state charge density at or near the interface.

c) Mobile and fixed ionic charges within the gate oxide.

d) The redistribution of impurities at the silicon surface during thermal oxidation.

1.3.1. Fast Surface States:

The energy levels of these states fall within

the silicon bandgap. The amount of charge in these

states is a function of the surface potential and

varies with the applied gate voltage.[25,26] These

are called "Fast Surface States", because these

charges can easily and quickly be exchanged with

the near-charges of the silicon substrate. The

origin of these states is the disruption of the

periodicity of the silicon lattice near the silicon-

silicon dioxide interface. It has also been found[27]

that the density of fast surface states is

the highest for (111) oriented silicon, and

the lowest for (100) oriented silicon, with

all other process conditions remaining the same.

These fast states act as scattering centers

at the silicon - silicon dioxide interface and

tend to reduce the effective carrier mobility in

the channel. This also results in increasing

the threshold voltage of the device. Castro and

Deal[28] showed that annealing at low temperatures

in an inert or reducing atmosphere (such as hydro-

gen or forming gas) reduces the density of these

states.

1.3.2. Fixed Positive Surface Charge Density, Q_{SS}:

This surface state charge in the silicon -

silicon dioxide interface was identified and

studied by Zaininger and others[29,30]. The energy

levels associated with these charges lie outside

the silicon bandgap. Unlike the fast surface

states, these charges are not dependent on the

surface potential or the applied gate voltage. But

the density is highest for (111) oriented silicon

and lowest for (100) orientation. Measurement of

Q_{SS} values has been made by using low frequency

capacitance-voltage methods[31] and conductance techniques[32]. The effects of processing on the value of Q_{ss} have been studied. The effects on Q_{ss} of oxidation temperatures and ambients have been presented by Deal and others[33,34]. The Q_{ss} values could be reproducibly reduced by annealing in a dry inert gas or in dry oxygen at an appropriate temperature.

1.3.3. Mobile and Fixed Ionic Charges:

Impurity ions of alkaline metals like sodium and those of hydrogen, all electropositive in nature, are known to be present in the oxide layer[35]. A radiochemical analysis technique of determining the distribution of sodium ions was described by Yon[36]. These ions are mobile in the oxide and they diffuse as well as migrate under temperature and electric field stresses[37]. Snow[38] introduced sodium and Lithium into the oxide and measured their transport as a function of time, temperature and voltage stress. Other studies have also been made on these ionic drifts by Goetzberger, Hofstein and others.[39,40,41,42] Frequent purging of the oxidizing tubes by HCl gas and dry oxygen and addition of HCl to the

oxidizing atmosphere are known to reduce the sodium contamination in the oxide.[43] Use of phosphosilicate glass over the oxide to getter the sodium ions is well known in the industry[44].

Ionizing radiation from γ-rays, X-rays and electron irradiations also affect the MOS devices[45]. When a positive or a negative bias is applied to the gate, there is a build-up of a space-charge region within the silicon dioxide. There is also an increase in the fast surface-state density due to these irradiations. These effects tend to shift the threshold voltage of the device under positive and negative gate bias and temperature stresses. Al_2O_3 is known to be more resistant to incident radiation as compared to SiO_2.

1.3.4. Impurity Redistribution During Thermal Oxidation:

During thermal oxidation at elevated temperatures, the different impurities commonly used to dope silicon tend to redistribute at the surface of the silicon substrate[46,47]. Boron tends to be depleted from the silicon surface, while phosphorus tends to pile up at the silicon

surface during oxidation, the concentration being

dependent on the oxidation temperature, and the

depth of redistribution into the silicon being

dependent on the oxidation temperature as well as

time.

1.4. Electromigration:

Revesz[48] has discussed the possible reactions

at the aluminum metal-SiO_2 interface, contributing

to metal ions which migrate into the oxide under

the influence of an electric field. This has

been further studied by Berger and others[49,50] in

detail. A comprehensive survey of the phenomenon

has been published by Black[51]. To obviate this

phenomenon, silicon gates to replace aluminum

gates have been developed[52].

1.5. Double-layer Gate Insulators:

Both silicon nitride and aluminum oxide are

known to be very effective barriers to sodium ion

migration in the presence of high electric fields[53].

The preparation and properties of silicon nitride

have been investigated in detail[54,55]. In order

to retain the highly desired properties of the

interface between silicon and thermal oxide and

at the same time prevent sodium ion migration, devices have been fabricated[56] using double-layer gate insulators. SiO_2 - Si_3N_4 and SiO_2-Al_2O_3 devices have been fabricated by manufacturers.

An additional advantage of these devices is the fact that Si_3N_4 and Al_2O_3 have much higher dielectric constants than SiO_2 and for the same mechanical thickness, these double-layer insulators will be electrically equivalent to a thinner layer of SiO_2. The threshold voltages can be made lower as required in integrated circuits, particularly when they are to be interfaced with bipolar integrated circuits. The properties of Metal-Nitride-Oxide-Semiconductor (MNOS) devices have been compared with those of MOS structures by several researchers.[57,58,59]

1.6. Self-aligned Gate Electrodes:

Conventional Silicon MOSFETs are not capable of operating at higher frequencies as compared to the capability of bipolar devices. In enchancement mode devices, there is no initial channel present with zero gate voltage and a conducting channel is formed only when the gate voltage of appropriate

polarity is applied. This feature necessitates the gate electrode to extend completely over the region between the drain and the source. In order that a slight misalignment of the gate electrode does not ruin the device, it is common practice to allow the gate electrode to overlap both the source and the drain electrodes. This overlap, coupled with the thinness of the insulating layer, gives rise to appreciable parasitic capacitances between gate and drain and gate and source. This provides a negative feed-back effect which increases with frequency. As a result, at higher frequencies gain drops off considerably, accounting for the poorer performance mentioned above.

In order to reduce the gate-to-drain and gate-to-source parasitic capacitances, "Self-aligned Gate Electrodes" have been developed and used. The most common material used for the self-aligned gate electrode is polycrystalline silicon[60,61], though molybdenum has also been used[62]. The polycrystalline silicon is first deposited over the gate oxide and then p or n type diffusion of the silicon substrate is done to form the drain and source regions. During the diffusion, the polycrystalline

silicon gate acts as a mask to prevent the
doping of the channel region. In addition,
the silicon gate itself gets heavily doped
to make it highly conductive, so that no metaliza-
tion is required except for contact.

Because of the difference in work function be-
tween aluminum and silicon, the threshold voltage
is lower for these devices. Since the gate is in
place prior to diffusion, tight tolerance is not
required for definition of the gate. In integrated
circuits, this allows a higher packing density
of components. Also, both poly-silicon and
aluminum layers can be used for interconnections
in integrated circuits[63].

1.7 Ion Implantation:

The development of ion implantation tech-
nology made it possible to control the threshold
voltage of MOS devices with great flexibility[64].
It is possible to obtain low threshold voltages
with p-channel devices. High energy ion accelera-
tors are used to implant dopant impurities into
the substrate, the source and drain regions, or
the channel region itself to control the threshold
voltage. It has been found[65] that it is possible

to shift the threshold voltage of both p-channel
and n-channel devices, by implanting a small concen-
tration of donor or acceptor impurities through
the gate region into the silicon substrate. In
the case of silicon-gate devices, the gate itself
acts as a mask to protect the underlying channel
region from implantation of dopant ions, while
the source and drain regions alone are doped
by implantation[66].

Ion Implantation and its ramifications have
been studied in detail by several research-
ers.[67,68,69,70]

1.8 Reliability of MOS Devices:

The reliability of semiconductor devices has been
stated[71] to be a function of the following:

        E - Electric Field

        S - Surface

        P - Package

        A- Ambients

        T- Temperature and Temperature Gradient

        X- Special Factors

The reliability factors with particular reference
to MOSFET's and Integrated Circuits, and micro-

electronics in general, have been expounded in detail.[72,73,74,75] Improvements in the reliability of integrated circuits have been outlined in a recent paper by Hawkins[76].

The various modes and failure mechanisms in MOS devices have been analyzed and presented in the literature.[77,78,79,80] The available techniques for failure analysis were summarized by Workman[81]. The use of electron microscopy for failure diagnostics[82] has become very extensive. Studies have been made of the failure modes at the surfaces and interfaces by Goetzberger and others.[83,84] The reliability factors involved in the aluminum metalization on the oxide have been identified[85].

The effects of long term storage on reliability of MOS devices have been presented[86] and the results of accelerated life tests on them published.[87,88]

1.9. Scope of this Investigation:

This investigation primarily concerns the threshold voltage of MOS devices and its stability. Under positive and negative gate biases at elevated temperatures, the ionic impurities in the oxide undergo transports and redistribute. This re-

distribution along with other factors makes the threshold voltage drift, thereby affecting the reliability of the device. These effects are studied in the investigation.

For purposes of this study, several MOS field-effect-transistors were put under various positive and negative gate biases and temperatures and life tested for several thousand hours. The threshold voltage of the devices were measured initially and at appropriate intervals, and the drifts analyzed. Theories have been developed to logically explain the results obtained.

CHAPTER II

BASIC THEORY OF MOSFET's

2.1. General:

The following discussion applies for a
p-channel device, and is applicable with necessary
minor modification to an n-channel device as
well. The mechanism of conduction is described
in detail, the threshold voltage V_T is defined,
and a mathematical expression for V_T is derived.
The importance of the stability of V_T is also
explained.

In a p-channel device shown in figure 1, the
semiconductor bulk material is n-type silicon,
and the mobile charge carriers deep in the bulk are
electrons. The insulating material on the surface
is silicon dioxide. The electrical condition
that characterizes the silicon at the surface* is
said to be accumulation, depletion, or inversion,
according to whether the mobile charge density at

---

* "The silicon surface is defined as that region of semi-
conductor material encompassing the outermost layer of
structural silicon atoms inward to that position within
the bulk interior where the energy bands become flat"[89].

G

Gate Electrode

D

Gate Oxide (SiO$_2$)

S

p   drain

source   p

Channel Region

n-type Silicon Substrate

n

ss
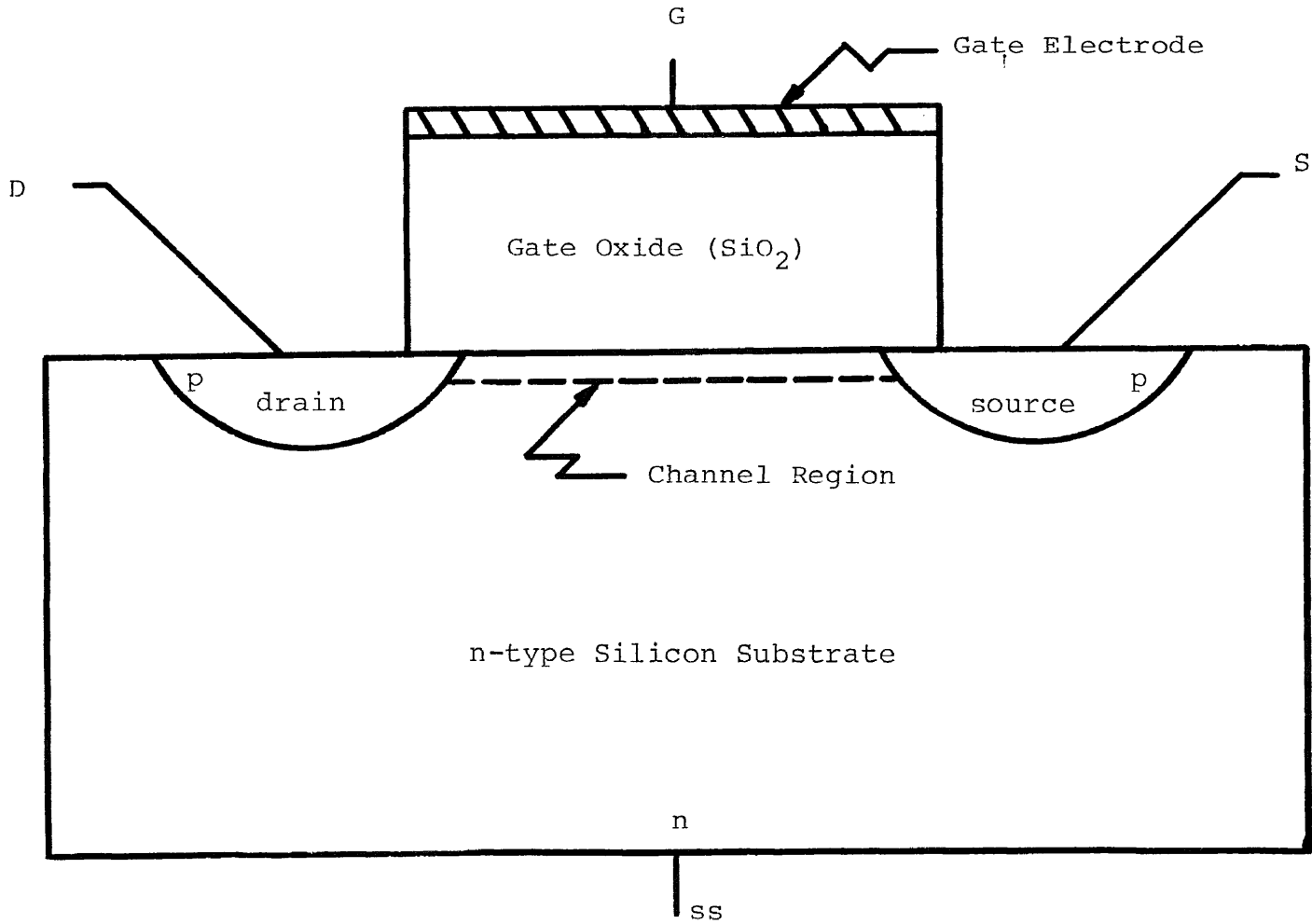
FIG 1.   P-Channel MOSFET Structure

the surface is greater than, less than, or of the
opposite type to that in the bulk silicon.

2.2. The Mechanism of Conduction in MOSFET's:

Figure 2a shows the energy band diagram
of the device with no gate voltage applied. A pos-
itive surface state charge $+Q_{SS}$ always exists in
thermally grown silicon dioxide[90]. Hence electrons
are attracted from within the n-type bulk and
accumulate at the surface. This results in the
downward bending of the conduction and the valence
bands as shown in the figure. In this and the
following diagrams, the intrinsic energy level E_i
is assumed to be midway between the conduction and
the valence bands, while the Fermi level E_F is shown
closer to the conduction band, as the material is
of n-type. The Fermi potential is also shown as $\emptyset_F$.
The charge density distribution, approximated by
δ functions is shown in figure 2b. The positive
surface charge density $+Q_{SS}$ is balanced by the nega-
tive charge density $-Q_A$ of the elctrons accumulated
at the silicon surface.

If a negative gate voltage is now applied to
the gate electrode (gate charge = $-Q_G$) such that it

Gate

Si Surface

$V_G = 0$

E_C

E_F

ϕF

E_i

E_V

a

$V_{G_1} < 0$

E_C

E_F

E_i

$\phi_S = 0$

E_V

c

ρ

Q_{SS}

Q_A

$Q_{SS} + Q_A = 0$

b

ρ

Q_{S_S}

Q_G

$Q_G + Q_{SS} = 0$

d
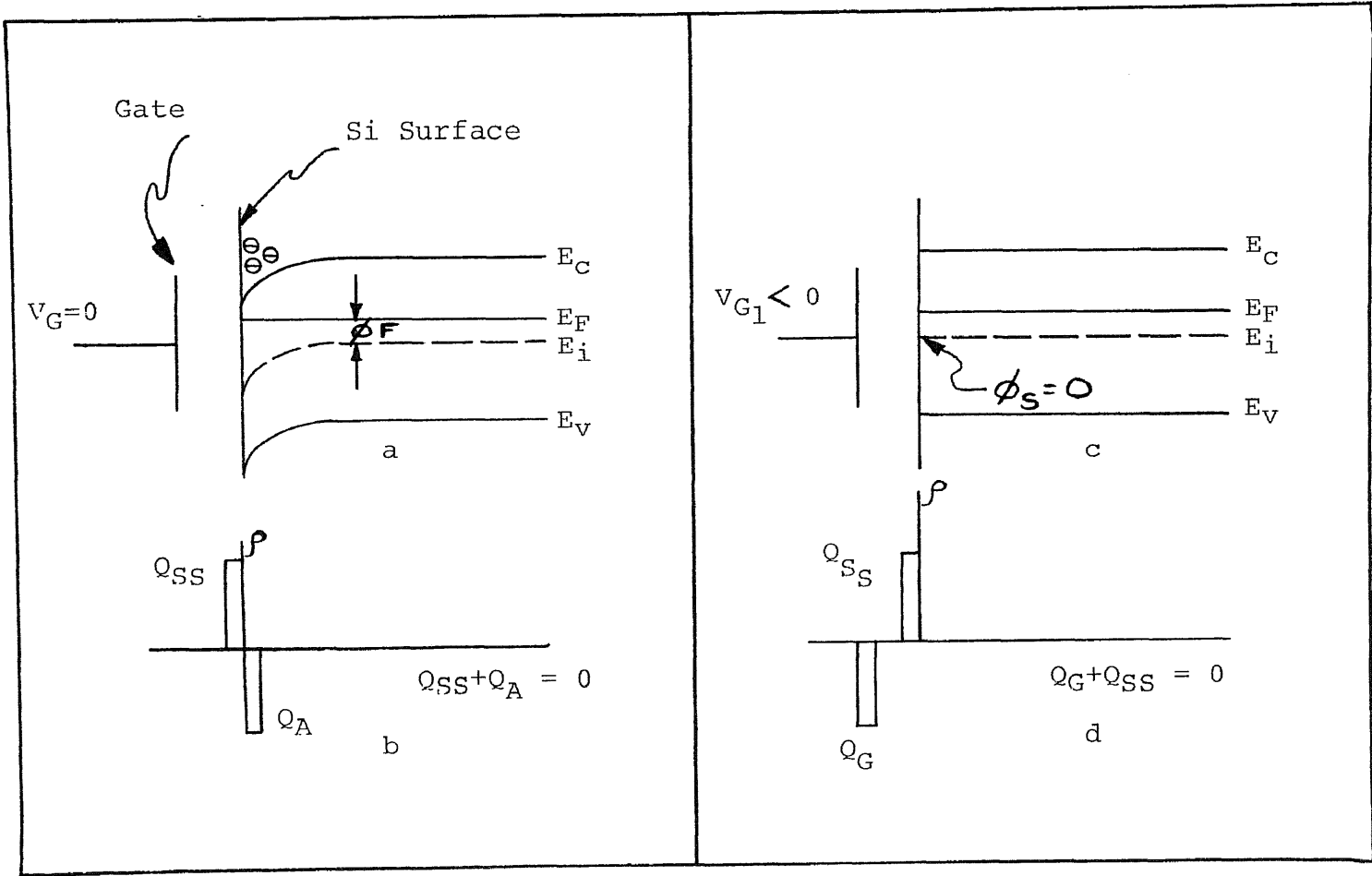
FIG 2.   Energy Band and Charge Distribution Diagrams

$V_{G2} < V_{G1}$

$\ominus$

$\phi_S = \phi_F$

E_c

E_F

ϕ_F

E_i

$\oplus$

E_v

e

ρ

Q_{SS}

Q_D

$Q_G + Q_D + Q_{SS} = 0$

Q_G

f

$V_{G3} < V_{G2}$

$\phi_S = 2\phi_F$

E_c

E_F

ϕ_F

E_i

$\oplus\oplus$
$\oplus\oplus$

E_v

g

ρ

Q_{SS}

Q_I

Q_D

$Q_G + Q_{SS} + Q_I + Q_D = 0$

Q_G

h
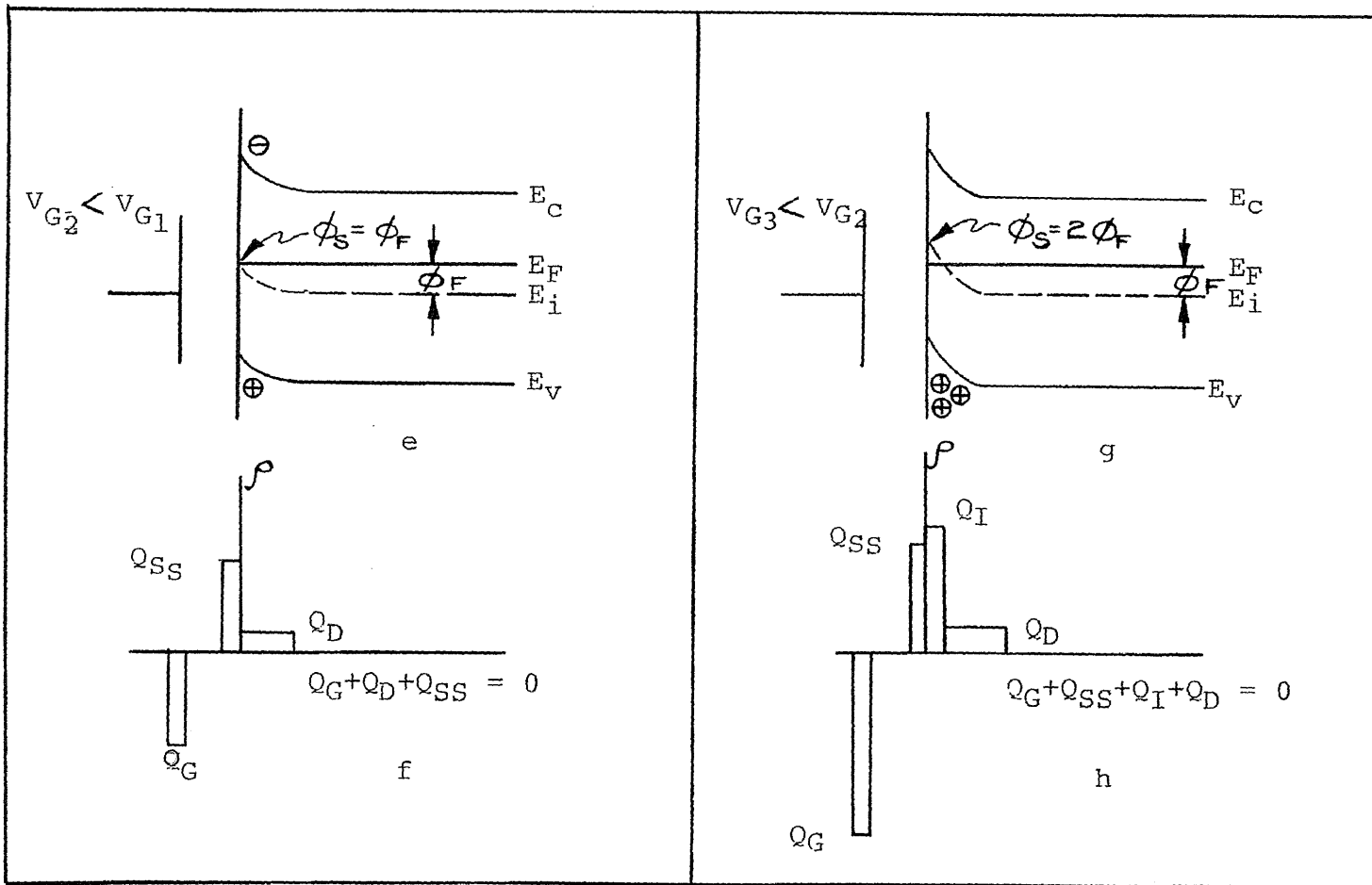
FIG 2. continued

just balances the effect of $+Q_{SS}$, the accumulation

of the electrons near the silicon surface disappears,

and there is no longer any bending of the bands.

The surface potential $\emptyset_S = 0$. This condition is

illustrated in figures 2c and 2d, and is known

as the flat band case.

If the negative voltage at the gate is further

increased, the mobile electrons at the donor centers

in the channel region are repelled, and a depletion

region is formed. The charge density $+Q_D$ in this

depletion region is hence positive. Figures 2e

and 2f depict the energy bands and the charge dis-

tributions respectively under these conditions.

When E_i is bent just sufficiently to intersect

E_F at the surface (such that $\emptyset_S = \emptyset_F$), the surface

has become intrinsic from its initial n-type concen-

tration. In other words, the mobile holes just

equal the mobile electrons at the surface. Under

this condition, the gate charge $-Q_G$ must just balance

out the surface state charge $+Q_{SS}$ and the depletion

region charge $+Q_D$.

When negative gate bias is still further in-

creased, mobile positive holes are attracted towards

the surface, and an increasing percentage of the

charge in the channel region is contributed by holes. At $E_i = E_F$, mobile electrons still outnumber holes in the channel region; but as the gate bias is made more negative, E_i rises above E_F at the surface and the density of holes becomes more than that of electrons. The surface is now said to be "inverted". When E_i is sufficiently greater than E_F at the surface to make $\emptyset_S = 2\emptyset_F$, the surface has become as much p in nature as the bulk is n. Under these conditions, conduction is deemed to have commenced between the source and the drain through the channel. In other words, the channel region has been inverted and has a positive charge density $+Q_I$. These conditions are shown in figures 2g and 2h.

The gate voltage at which the conduction thus commences is called the "Threshold Voltage" of the device*. Or, the threshold voltage is that voltage at the gate that produces a gate charge $-Q_G$, just sufficient to counteract the surface state charge $+Q_{SS}$, and the charge $+Q_D$ of a depletion region that supports a potential of $2\emptyset_F$.

---

* A practical engineering definition of threshold voltage is given in section 4.1. See also Appendix G

To summarize, in order to effect conduction in a p-channel device, a sufficiently negative gate voltage must be applied so as to produce enough negative gate charge $-Q_G$ to

i) counteract $+Q_{SS}$ and undo the accumulation of electrons at the surface.

ii) repel mobile electrons from the donor centers in the channel region.

iii) attract into this region sufficient number of mobile holes, so that the number of holes dominate over the number of electrons. (i.e.) to invert the channel region into a p region.

Finally, it is appropriate to remark that the onset of conduction is a gradual process of transition from depletion to inversion, during which there is a continuous increase of hole concentration in the channel region, as the electron concentration simultaneously and continuously decreases.

2.3. Expression for Threshold Voltage:

Based on the discussion in the previous section, an expression for the threshold voltage can easily be derived. Let the terms be defined as below:

V_T - threshold voltage of the device

Q_G - charge density on the gate metal

Q_{SS} - surface state charge density at the silicon-silicon dioxide interface

Q_B - charge density in the bulk

$\rho(x)$ - impurity ion density at a distance x

from the gate electrode (see figure 3)

t_{ox} - thickness of the gate oxide

ε_{ox} - relative permittivity of silicon dioxide

ε_o - absolute permittivity of vacuum

ϕ_{MS} - work function difference between silicon and the gate metal

The algebraic sum of all the charges in the MOS system should be zero. The gate oxide region of the MOS system constitutes in effect a capacitor, charged by the voltage applied to the gate metal. Under threshold conditions, the charge on this capacitor per unit area is

$$Q_G = V_T \left(\frac{\varepsilon_o \, \varepsilon_{ox}}{t_{ox}} \right)$$

For total charge neutrality,

$$Q_G + Q_{SS} + Q_B = 0$$

Therefore,

$$V_T \left(\frac{\varepsilon_o \, \varepsilon_{ox}}{t_{ox}} \right) + Q_{SS} + Q_B = 0$$

If an additional charge in the oxide contributed by a distributed impurity ion density $\rho(x)$ as shown in figure 3 is considered,

$$V_T \left(\frac{\varepsilon_o \, \varepsilon_{ox}}{t_{ox}} \right) + Q_{SS} + Q_B + \int_o^{t_{ox}} \frac{x}{t_{ox}} \rho(x)\,dx = 0$$

Note that the fourth term in the above expression is obtained by considering the distributed impurity
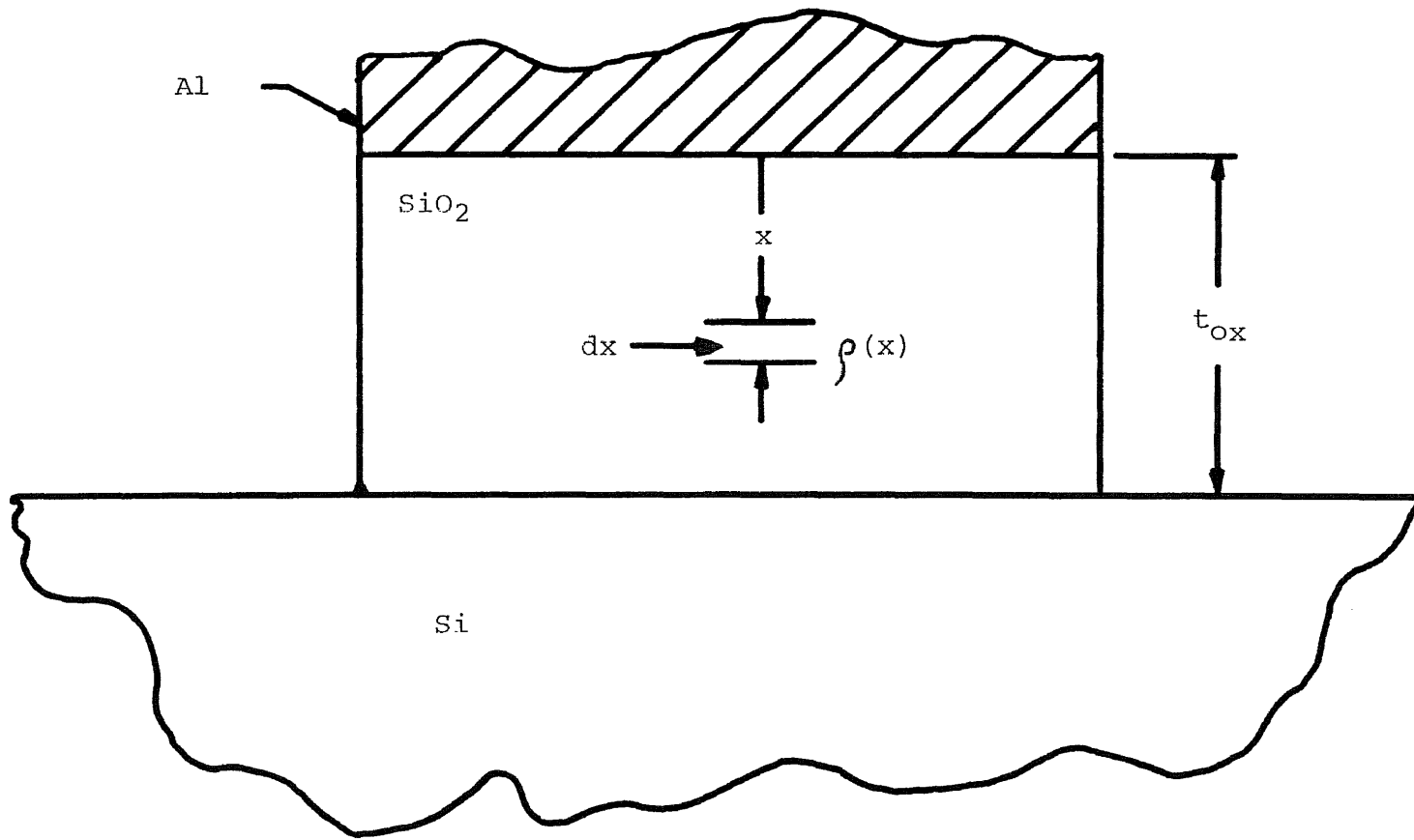
FIG 3. Impurity Ion Charge Density Distribution

ion density as an equivalent charge density located
at the gate electrode.

The above equation can now be rearranged and
written conveniently as

$$V_T = - \left[\frac{Q_{SS} + Q_B + \int_o^{t_{ox}} \frac{x}{t_{ox}} \rho(x) dx}{\mathcal{E}_o \mathcal{E}_{ox}/t_{ox}} \right]$$

Finally, if the gate voltage necessary to counter-
balance the work function difference between the
gate metal and the silicon substrate is also
considered, the expression for the threshold volt-
age stands modified as below:

$$V_T = - \frac{Q_{SS} + Q_B + \int_o^{t_{ox}} \frac{x}{t_{ox}} \rho(x) dx}{\mathcal{E}_o \mathcal{E}_{ox} / t_{ox}} + \emptyset_{MS}$$

2.4. Importance of Threshold Voltage Stability:

The drain characteristics of a typical p-channel
MOSFET is shown in figure 4. The drain current I_{DS}
is plotted against the drain voltage V_{DS}, for
different constant values of the gate voltage V_{GS}.
It can be split into three regions of operation.
In region 1, V_{DS} values are very low, and I_{DS} in-
creases linearly with V_{DS}. Region 2 corresponds to
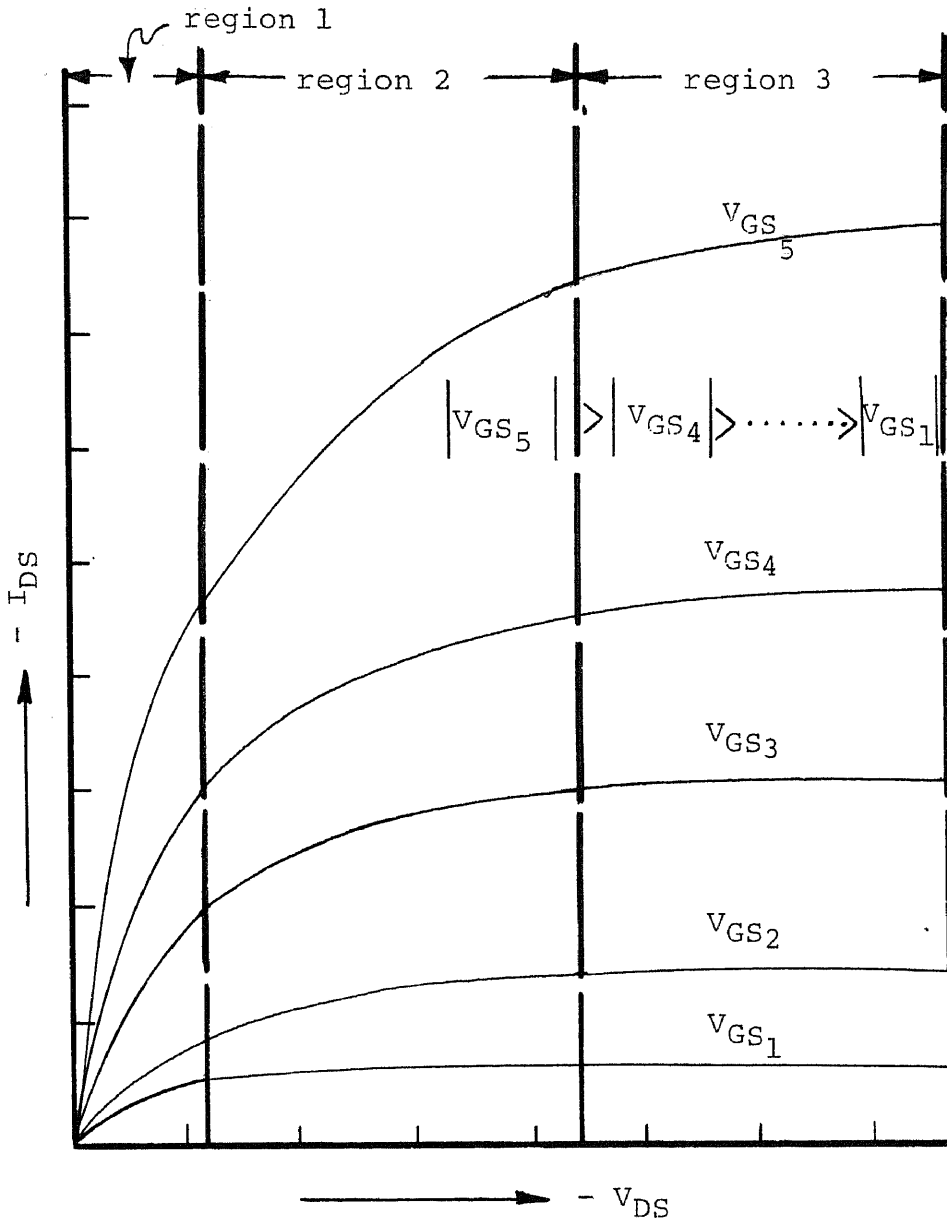
FIG 4. Drain Characteristics of a P-Channel MOSFET

higher values of V_{DS}, but saturation has not commenced. In this region, I_{DS} can be expressed[91] approximately as:

$$I_{DS} \simeq -K \left\{ (V_{GS} - V_T) V_{DS} - \tfrac{1}{2} V_{DS}^2 \right\}$$

$$\left[K = \mu_p \; c_{ox} \; \tfrac{w}{l} \right]$$

where μ_p = average mobility of holes in the channel

c_{ox} = oxide capacitance

w = width of the channel

l = length of the channel

In region 3, saturation sets in and I_{DS} is given by the expresion

$$I_{DS} \simeq - \frac{K}{2} (V_{GS} - V_T)^2$$

In amplifier applications, the load line is so set to have the operating point well into the saturation region. The transconductance g_m in this region can be derived as shown below:

$$g_m = \frac{\delta I_{DS}}{\delta V_{GS}} \bigg|_{V_D} = \frac{\delta}{\delta V_{GS}} \left[- \frac{K}{2} (V_{GS} - V_T)^2 \right]$$

$$= - K(V_{GS} - V_T)$$

From the above expression, it can be seen that any drift in V_T will correspondingly alter g_m, thereby affecting the circuit operation, unless the circuit

is designed taking this into account.

In switching circuits, the instant of turn-on, when conduction commences, is directly dependent on V_T. So any drift in V_T tends to affect switching directly.

CHAPTER III

CONSTRUCTION AND RELIABILITY FACTORS

3.1. Construction:

The discussion here will be confined to the
p-channel device, which is fabricated from a thin
single crystal n-type substrate. Silicon crystal
growth is the first step. The crystal is pulled from
molten silicon containing an appropriate concentra-
tion of a n-type dopant, usually phosphorus. The
crystal orientation commonly used is either (111)
or (100), and this orientation is identified by
providing a flat in the cylindrical ingot rod. The
rod is then "zone-cut" into different resistivity
ranges. The appropriate resistivity range selected
for the MOSFET fabrication is then sliced into thin
wafers about 8 mils thick, the thickness just suffic-
ient to handle without breakage in subsequent process-
ing. These wafers vary in diameter from an inch to
several inches.

The wafers are then checked for substrate dis-
locations, so as to ensure proper oxide growth in
later processing. They are then lapped and polished
to a high degree, in order that the carrier traps
may be minimized[92].

The typical "thick oxide" process discussed hereunder has about 15,000 angstroms thick final oxide over the diffused p-regions.

The wafers are first thoroughly cleaned before initial oxidation. They are then placed on a quartz boat and loaded into the open-ended quartz tube of an oxidation furnace held at a controlled temperature (900°C to 1200°C). An oxide layer of 5000 to 6000 angstroms thickness is grown as shown in figure 5a. This oxide acts as a mask against subsequent diffusion.

After initial oxidation, comes the first masking step. Liquid photoresist is spin-coated on the wafer, which is baked to remove the resist solvents. An appropriately designed mask is applied and exposed to a light source. The photo-resist is further developed by dipping in a suitable solvent. After a second bake to drive off the residual developer, the oxide is selectively etched with a solution of hydrofluoric acid and ammonium fluoride. The mask pattern used in this step is to define the source and drain regions, and to etch off the oxide in those defined regions (see figure 5b). This operation determines the critical source-to-drain length, and must be

Initial Oxidation

a

1st Etch for Source
and Drain Diffusion

b

Pre-deposition

c

Diffusion and
Reoxidation

d

2nd Etch for Gate
Oxide

e

Grow Gate Oxide

f

3rd Etch for Contact
Metalization

g

Metalization

h
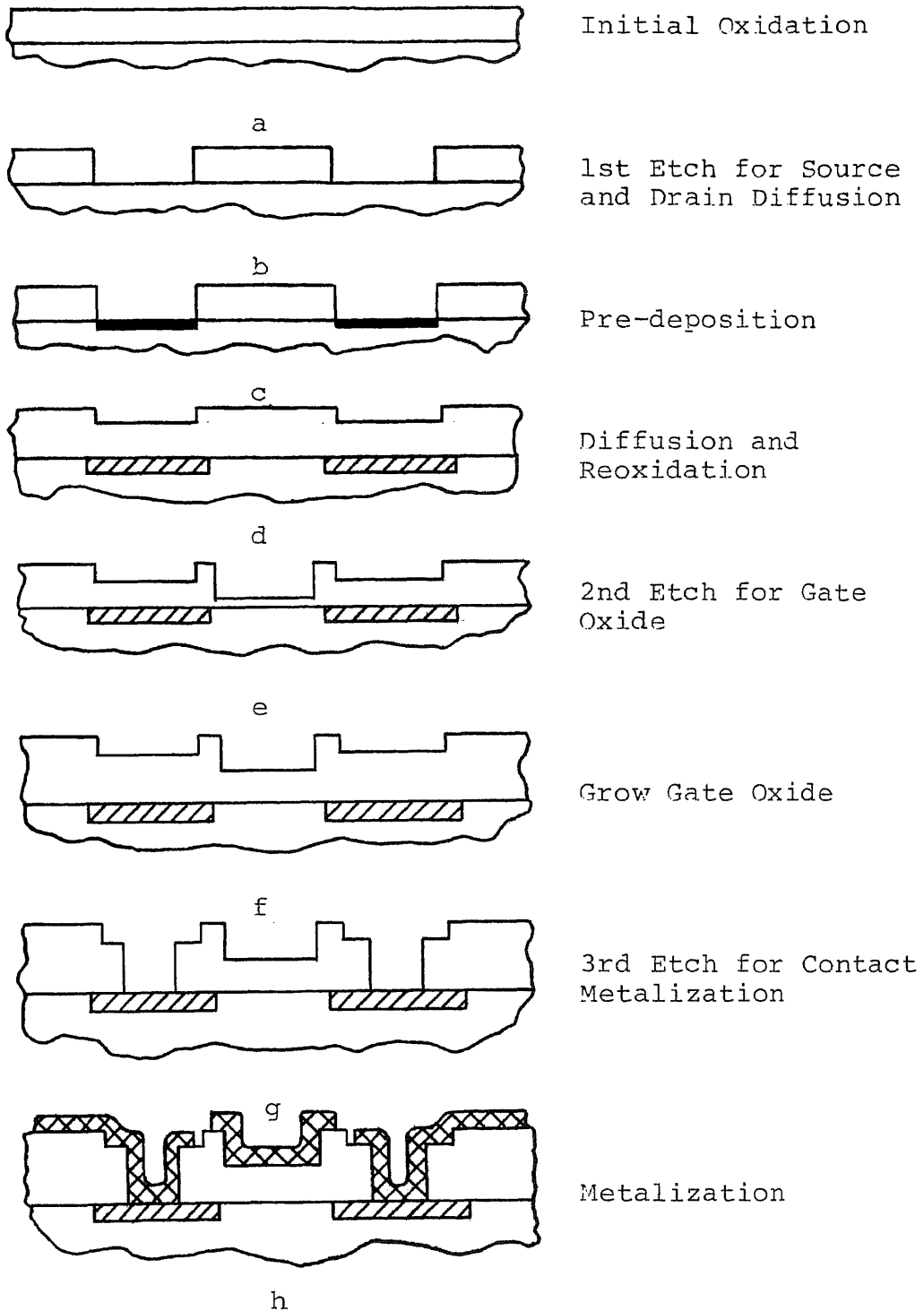
FIG 5. Thick Oxide Process Steps

tightly controlled.

The next step, namely the p-diffusion of the source and the drain, is effected in two stages (figure 5c and 5d). In the first stage, a layer of the p-type impurity (usually boron) is deposited on by placing the wafers in a predeposition furnace tube (at $1000^{\circ}C$ to $1100^{\circ}C$) using an appropriate source like diborane (B_2H_6) or boron trichloride (BCl_3). In the second stage, the wafers are transfered to a driving furnace, where the p-type dopant impurity is diffused into the silicon to form the drain and source regions. A thick oxide layer of about 15,000 angstroms is again grown over the surface.

By using a second mask (gate mask), followed by an etching operation, substantially the entire thickness of the oxide at the gate region is etched off as shown in figure 5e. A small amount of over-lapping of the source and the drain regions by the gate is designed into this mask. The wafer is now ready for the gate oxidation, which is done usually in a dry oxygen atmosphere in an oxidation furnace at an appropriate temperature. The gate oxide grown is typically about 1,500 angstroms thick. This step is shown in figure 5f.

A third photo-masking and etching step is
performed as shown in figure 5g, in order to remove
the oxide over the drain and source regions, so
that contact metalization can be done. Aluminum
is the most common metalization used. Ultrapure
film of aluminum, 5,000 to 10,000 angstroms
thick, is evaporated on the wafer by using an
evaporater usually of the electron beam type.
This contact metalization is shown in figure 5h.

Finally, the finished wafer is sintered at an
appropriate temperature to ensure proper alloying of
the aluminum with the silicon so as to make the
contact resistance as low as possible.

It can be noted that since (100) oriented
silicon typically gives lower Q_{SS} values as compared
to (111) oriented silicon, lower threshold voltage
values can be obtained with the (100) orientation.
However, as the field oxide threshold voltage is
also correspondingly reduced, compensatory measures
such as increasing the field oxide thickness have
to be taken.

After aluminization, very often the wafers go
through a glass passivation step. A layer of
amorphous SiO_2, about 5,000 angstroms thick is vapor

deposited on top of the aluminum. This is usually
done at 300° to 500°C, temperatures much lower than
the melting point of aluminum, in a resistance heat-
ed reactor using silane (SiH_4) and oxygen as the
reactants. Another photomasking and etching oper-
ation is required to remove this oxide from the
bonding pad areas, before the wafers are ready for
assembly.

3.2. Reliability Factors:

Some of the reliability factors involved in the
fabrication of MOS devices are described below:

1. The thick oxide method described in section
    3.1 reduces the possibility of pinholes in
    the oxide. Apart from the thickness of the
    oxide, it can be noted that all areas, except
    where the gate overlaps the source and the drain,
    the oxide has been grown in two layers. This
    minimizes the propagation of pinholes complete-
    ly through the oxide.

2. A very high degree of polish in the lapping
    operation is essential. Since the MOSFET is a
    surface-controlled device, carrier traps should
    be reduced to a minimum. This is ensured by
    making the surface as evenly flat as possible by

polishing.

3. Proper alignment of masks used in the photoresist and etching operations is critically important. Frequent replacement of photomasks is mandatory. It is common practice in the industry to replace masks after 10 to 15 uses.

4. Super clean conditions, particularly in the photoresist and diffusion areas, are essential. Dust-free dehumified air flow, use of laminar flow hoods, use of pure deionized water in the cleaning operations, use of high purity "electronic" or "reagent" grade etchant solutions, and prevention of contamination from extraneous sources including the operating personnel are very important.

5. Before the aluminum metalization is done, it is good practice to etch off 50 to 150 angstroms of the gate oxide, in order to remove any sodium contamination due to the photoresist residues.

6. The electron beam evaporater for metalization is preferred, as it gives cleaner metalization free from alkaline ion contamination. In order to ensure uniform thickness of deposited aluminum,

special fixtures have been designed to

planetarily rotate the wafers, so as to provide

varying angles of incidence between the wafers

and the evaporater source.

7. Where stepping of the oxide is involved under

the metalization, they are appropriately sloped

to ensure that metalization cracks do not develop,

creating a reliability problem due to reduced

crosssection of metalization.

8. Passivation of the wafer surface greatly helps

in eliminating or at least, minimizing the

possibilities of scratches on the metalization, in

addition to reducing surface ion migration. The

presence of a small amount of phosphorus oxide

in the passivating layer acts as a "getter" to

trap and immobilize alkali ions, which contribute

to instability.[93]

9. Over-alloying of aluminum into base silicon on the

p-region contact cutouts should be avoided.

Though this alloying is done by sintering at closely

controlled temperatures, further alloying does

occur in several subsequent operations such as

die-attaching, wire-bonding etc., where temperatures

about $400^{\circ}C$ are used. The time duration for which

the die is exposed to this temperature
during assembly should be minimum, subject
of course to the requirements of good die-
attach and wire-bond. For the same reason,
ultrasonic wire-bonding is preferred to
thermocompression bonding.

10. Freedom from contamination is as important
for the package as it is for the die. The
package bases as well as caps should be effect-
ively cleaned before use in the assembly line.
Between such cleaning and their actual use in the
assembly, they should be stored under clean and
inert conditions.

3.3 Gate Protection:

The fact that the gate of a MOSFET acts as a
capacitor makes the device very sensitive to damage
by stray electrostatic charges, that can be generated
during normal handling. A typically 1500 Angstroms
thick gate oxide would require at most 150 volts
to break down, assuming a high quality oxide with a
breakdown strength of 10^7 volts/cm. Assuming a gate
capacitance of 4 pf, this voltage would need only a
small charge of (4×10^{-12}) (150) Coulomb or 0.6
nCoulomb. Hence protective devices are very often

incorporated into the construction of MOS devices.

The most common form of protection is a diffused diode in parallel with the gate[94]. The breakdown voltage of this diode is designed to be just above the maximum operating gate voltage of the device. Its dynamic resistance in breakdown should also be low. Another form of protection is the incorporation of also a diffused resistor in series with the gate, which helps to limit the current during breakdown[95].

3.4 Reliability Assurance Methods:

In conjunction with production, it is also important to provide reliability assurance. Most quality assurance specifications include references to the following documents:

    MIL - STD - 883A   Test Methods and Procedures for
                       Microelectronics.

    MIL - M - 38510   Microcircuits, General Specifications for.

Uniform methods for testing are established by MIL - STD - 883A. These tests include environmental, mechanical, and electrical screening tests. A typical screening procedure is shown in tabular form in Appendix A.

3.5 Failure Modes and Analysis:

Some of the common modes of failure of MOS devices are listed in Appendix B. These include wafer-processing and assembly related failures, mechanical defects, and surface failures.

Failure analysis is a useful tool to discern from the failed unit the extent of its deterioration and cause of failure, so that corrective measures to improve reliability can be instituted based on the study. The proper sequence of individual tests is very critical, in order not to destroy evidence. The recommended sequence of individual steps and a summary of basic failure analysis techniques are given in Appendix C and Appendix D respectively.

CHAPTER IV

EXPERIMENTAL PROGRAMS AND TEST RESULTS

4.1. Engineering Definition of Threshold Voltage:

As explained in chapter II, section 2.2, the
threshold voltage of a p-channel enhancement mode
MOSFET is the gate voltage required for the onset
of conduction from source to drain through the
inverted channel. For practical measurement
purposes howver, engineering practice more specific-
ally defines the threshold voltage (V_T) for
p-channel devices as the gate-to-source voltage
(V_{GS}) required to generate a drain-to-source
current (I_{DS}) through the channel of a specified
value, under the condition $V_{DS} = V_{GS}$ (i.e. with
the drain and gate terminals connected together).
The specified I_{DS} value for the devices tested in
this study was -10uA.

4.2. Measurement of Threshold Voltage:

The circuit used for the measurement of thres-
hold voltage is shown in figure 6. A General Radio
D.C. amplifier and electrometer, type 1230A, was
used for monitoring the drain current, while a
Hewlett Packard A.C. - D.C. differential voltmeter,

Circuit for Measurement of Threshold Voltage
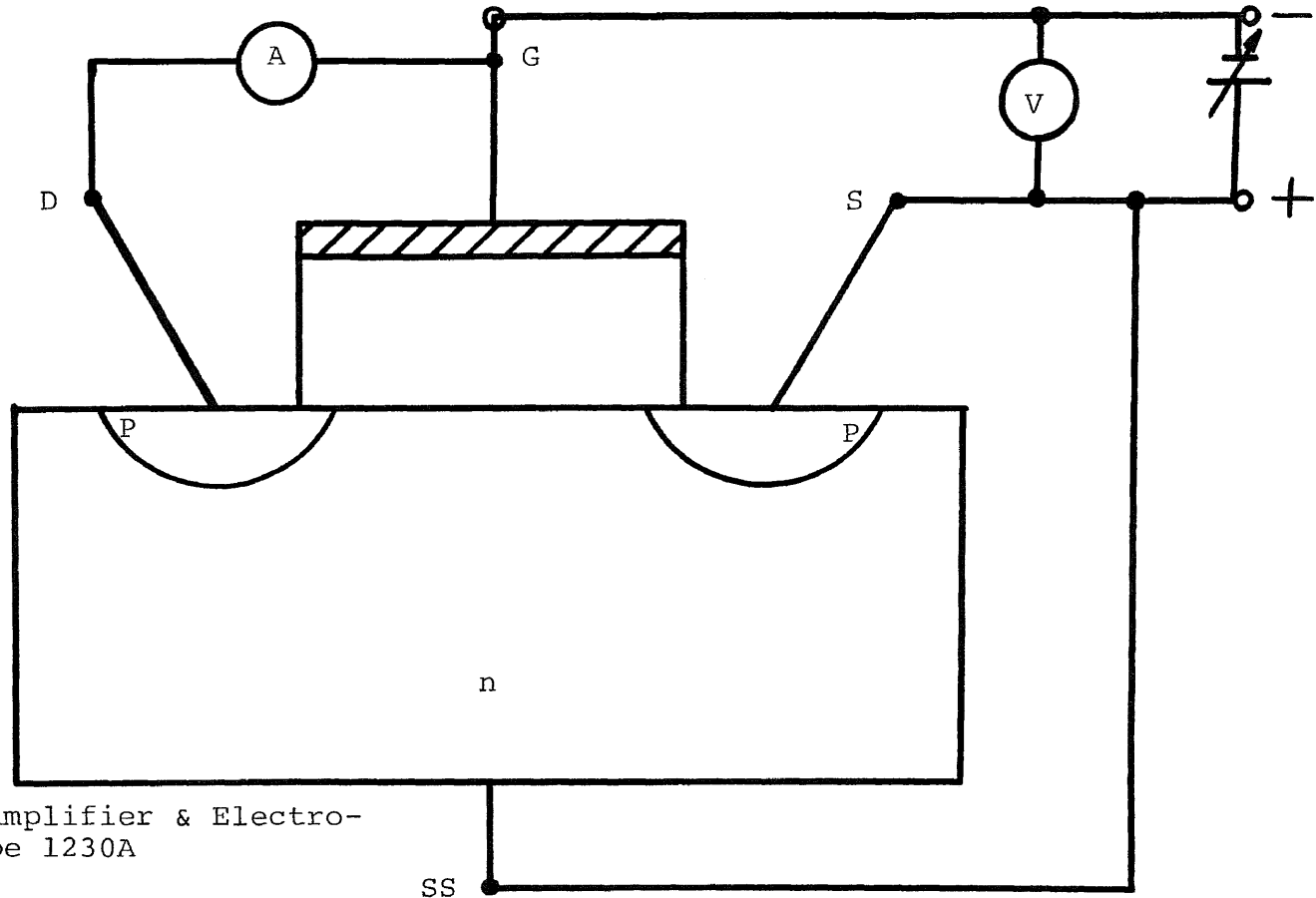
A GR D.C. Amplifier & Electro-
meter Type 1230A

V H.P. A.C.-D.C. Differential
Voltmeter Model 741A

FIG 6.

$$V_T = V_{GS} \text{ for } I_{DS} = -10uA$$
$$\text{at } V_{DS} = V_{GS}$$

model 741A, was used to measure the threshold
voltage. The latter instrument enabled the
measurement of V_T upto the 4th decimal (0.1 mV).

As already explained in Chapter III,
section 3.3, the inadvertent application of even
a small electrostatic charge to the gate of an
MOS device can cause a large enough voltage
gradient in the gate oxide to damage it. Hence
extreme precautions were taken in handling these
devices. A metal wrist strap connected to a
good ground connection was worn by the operator
while taking measurements. When the devices were
not under test, they were always kept with all
leads connected together to avoid any possible
damage, unless otherwise required.

4.3. Experimental Program:

Several p-channel MOSFETs were put under life
test under different high temperature stresses as
well as temperature and bias stresses for several
thousand hours. The threshold voltages were
measured initially and at appropriate intervals of
time. Their means and standard deviations were
calculated and the drifts in threshold voltage
with time studied and analyzed. Special care was

taken to ensure the accuracy of measurements. The several categories of life tests undertaken and the results obtained therefrom are explained in the following sections.

The devices used for the tests were DD07P, DD08P, and DD08K type MOSFETs, manufactured by American Microsystems Inc. These 3 types were of identical construction and ratings, except that DD07P had a protective gate zener, absent in the DD08P and DD08K types. The detailed specifications of these devices are given in appendix E.

4.4. High Temperature Life Tests:

97 DD07P type devices were used for these tests. The different storage temperatures and the number of devices under each condition are listed below:

Category	Storage Conditions	# of Devices
Ia	Temperature of $80^O \pm 3^O$C with all leads tied together	40
Ib	Temperature of $100^O \pm 3^O$C with all leads tied together	40
Ic	Room temperature ($22^O \pm 2^O$C) with all leads tied together	17
	TOTAL........	97

These life tests were carried out upto
15,000 hours, and V_T measurements were taken
at peiodic intervals. A summary of the data
is presented in table I (A & B), and charts I&II.
The drift from 0 hours to 15,000 hours in the
mean value as well as the standard deviation of
the threshold voltage of the units of all these
three categories were well under 1%, and hence
considered insignificant.

4.5. High Temperature and Negative Bias Life Tests:

A second group of 235 devices, consisting of
98 DD08P units and 137 DD08K units, were used
for these tests. The life test conditions and
quantities were as shown below:

Category	Storage Conditions	# of Devices DD08P	DD08K
IIa	Room temperature ($22^O \underline{+} 2^O C$) with all leads tied together	20	26
IIb	Temperature of $140^O C \underline{+} 5^O C$ with all leads together	40	55
IIc	Temperature of $140^O C \underline{+} 5^O C$ Bias $V_{GS} = -56V$; source, drain, and substrate tied together	38	56
	TOTAL......	98	137

TABLE I

DATA SUMMARY OF HIGH TEMPERATURE LIFE TESTS

A) Mean of $\left|V_T\right|$:

HOURS	CATEGORY Ia (80°C)	CATEGORY Ib (100°C)	CATEGORY Ic (Room Temp.)
0	4.8637	4.8363	4.7646
250	4.8405	4.8315	4.7362
500	--	4.8291	--
750	4.8606	4.8257	4.7653
1000	4.8571	4.8379	4.7539
1500	4.8521	4.8394	4.7536
2000	4.8559	4.8307	4.7656
3000	4.8597	4.8334	4.7765
4000	4.8531	4.8318	4.7598
5000	4.8533	4.8261	4.7545
7000	4.8363	4.8165	4.7468
10000	4.8505	4.8190	4.7626
12000	4.8646	4.8343	4.7685
15000	4.8469	4.8065	4.7493

TABLE I (continued)

B) Standard Deviation of V_T :

HOURS	CATEGORY Ia (80°C)	CATEGORY Ib (100°C)	CATEGORY Ic (Room Temp.)
0	0.1530	0.1678	0.2852
250	0.1497	0.1640	0.2785
500	--	0.1609	--
750	0.1478	0.1612	0.2792
1000	0.1482	0.1599	0.2765
1500	0.1495	0.1602	0.2770
2000	0.1491	0.1595	0.2773
3000	0.1496	0.1628	0.2792
4000	0.1549	0.1625	0.2876
5000	0.1540	0.1647	0.2869
7000	0.1537	0.1632	0.2887
10000	0.1538	0.1630	0.2868
12000	0.1569	0.1627	0.2870
15000	0.1558	0.1638	0.2881
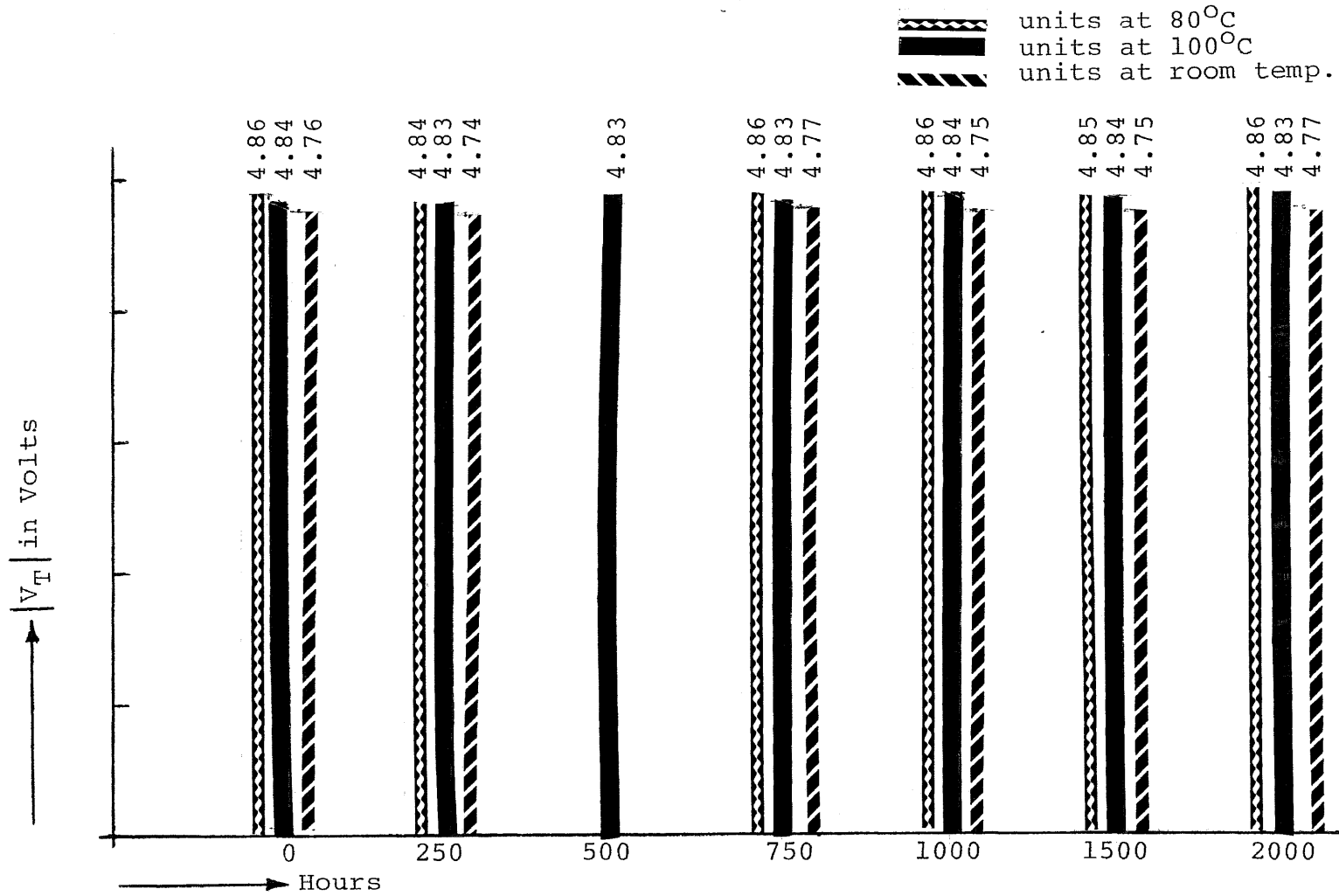
Chart I.   Mean of Threshold Voltage - AMI DD07P MOSFET's
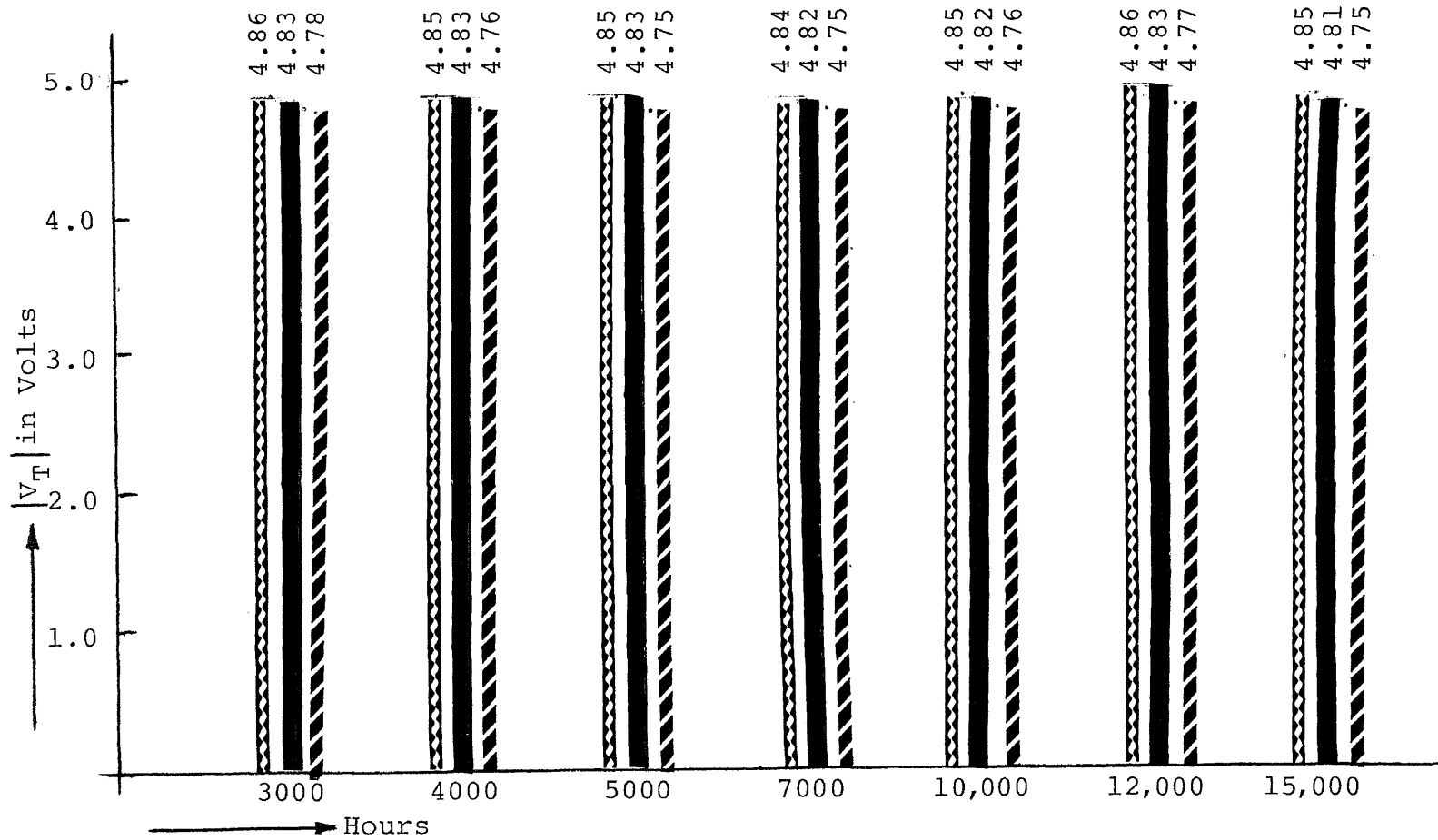
Chart I. continued
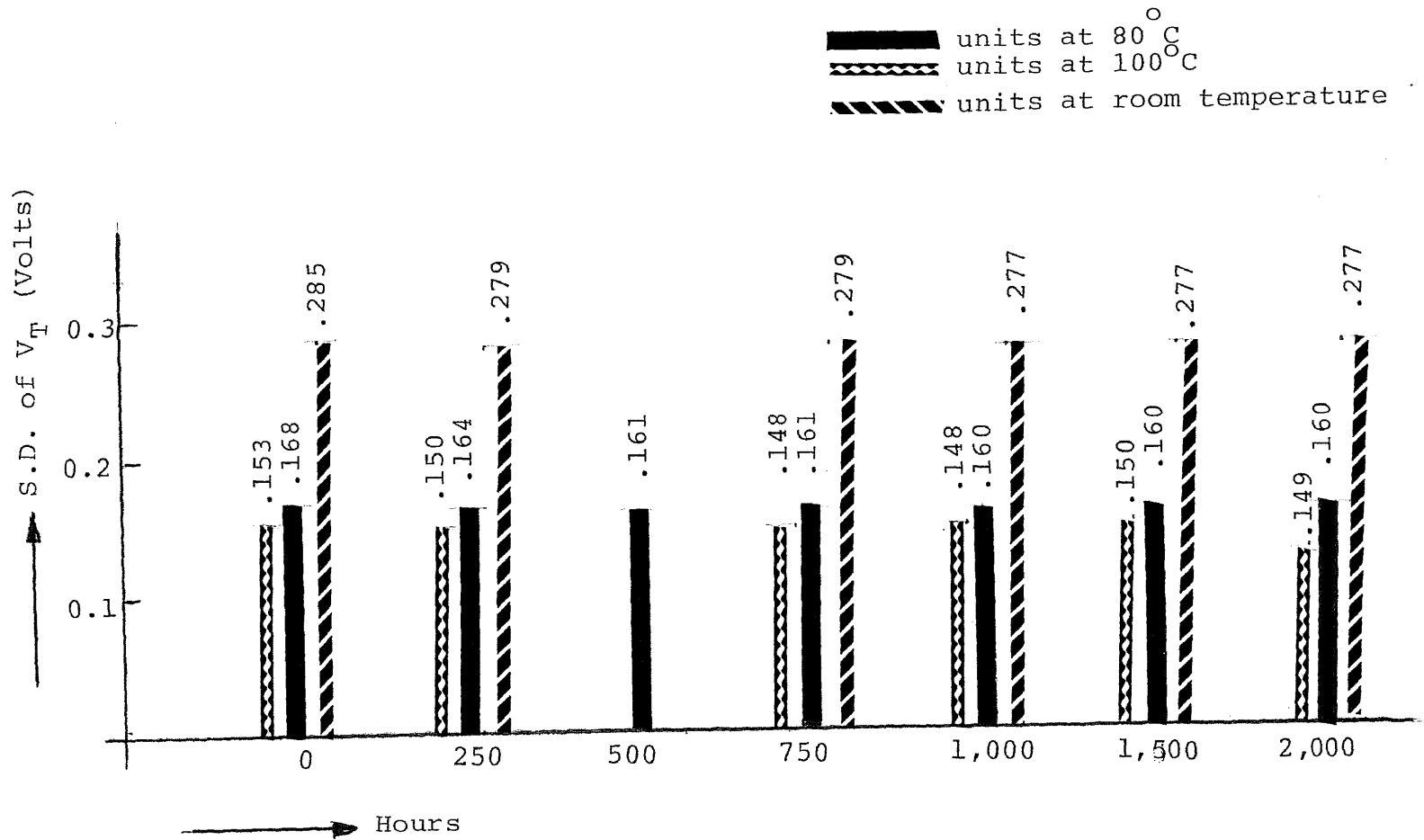
Chart II. S.D. of Threshold Voltage - AMI DD07P MOSFET's
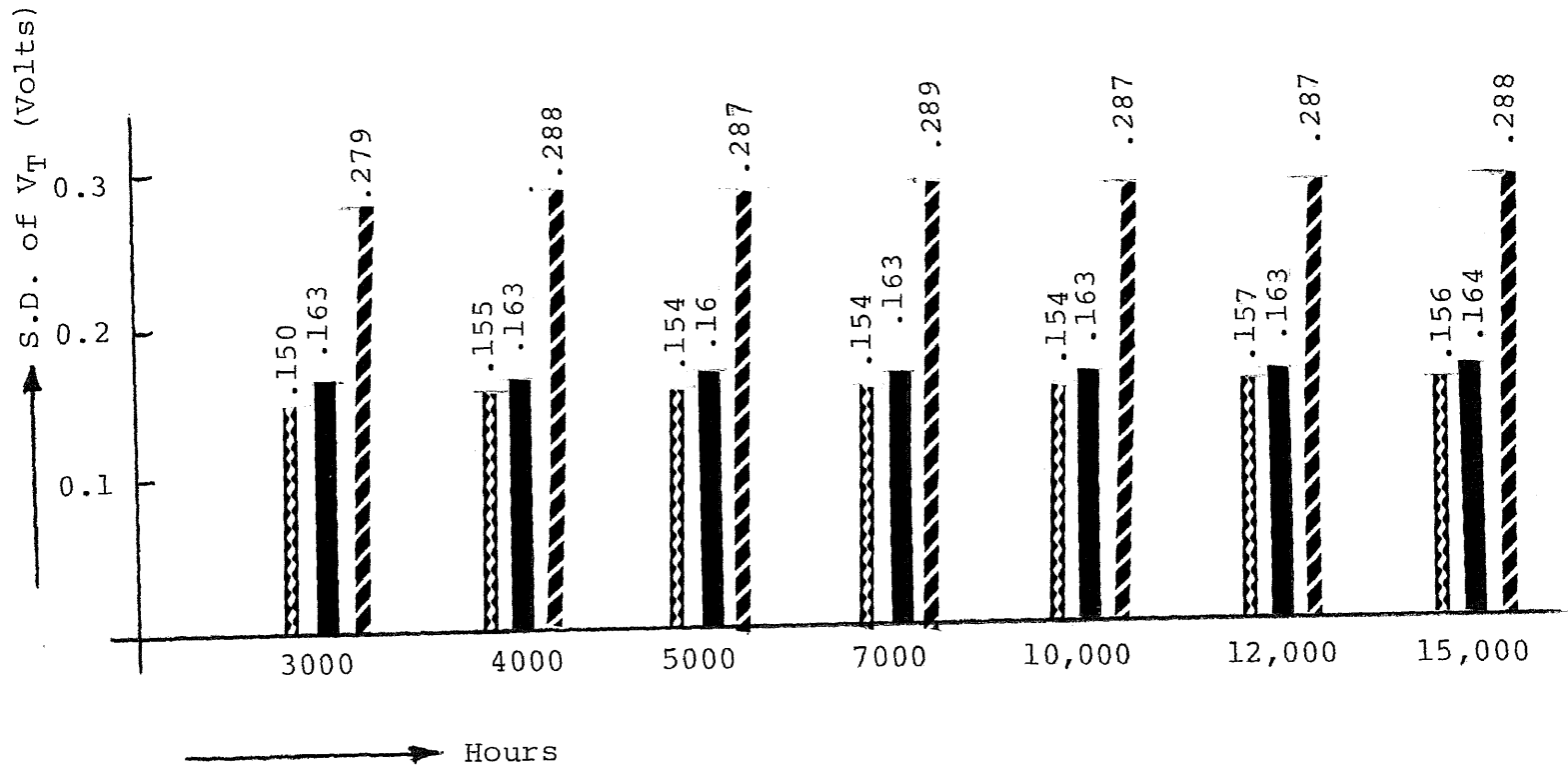
Chart II - continued

The gate bias of 56V on the IIc devices was 80%

of the maximum rating.   Since the gate oxide thick-

ness was about 1300 Angstroms, it corresponds to

an electric field of about 4.3×10^6 V/cm.

The results of these tests are summarized

in table II (A & B) and charts III & IV. The IIc

units were unable to withstand the high temperature

and negative gate bias and increased in mean thres-

hold voltage within 1100 hours by as much as 16%

and 18.8% for the DD08P and DD08K types respectively.

Hence these devices were removed from test at 1100

hours. However the IIa and IIb units were continued

on test upto 3100 hours. The drift in mean thres-

hold voltage of the IIa units at room temperature

was very insignificant. The IIb units at $140^{O}C$

decreased in mean threshold voltage by 1.4% and

5.4% respectively for the DD08P and DD08K types.

4.6. High Temperature and Positive and Negative Bias

Tests:

In the light of the results obtained on

the tests described in section 4.5, it was felt

that a lower gate bias with the same temperature

will yield more meaningful data, and that comparative

TABLE II

DATA SUMMARY OF HIGH TEMPERATURE AND NEGATIVE BIAS LIFE

TESTS

A) Mean of $\left|V_T\right|$:

HOURS	DD08P MOSFET's		
	Category IIa (Room temp. & no bias)	Category IIb (140°C & no bias)	Category IIc (140°C & V_{GS} = -56V)
0	4.2755	4.3412	4.2988
1100	4.2695	4.3018	4.9847
2100	4.2928	4.2914	--
3100	4.2846	4.2795	--
DD08K MOSFET's			
0	4.3353	4.4932	4.3957
1100	4.3013	4.3593	5.2215
2100	4.3422	4.2660	--
3100	4.3527	4.2488	--

TABLE II - continued

B) Standard Deviation of V_T :

HOURS	DD08P MOSFET's		
	Category IIa (Room temp. & no bias)	Category IIb (140°C & no bias)	Category IIc (140°C & V_{GS} = -56V)
0	0.1631	0.1544	0.1741
1100	0.1617	0.1632	0.1219
2100	0.1586	0.1825	--
3100	0.1595	0.1764	--
	DD08K MOSFET's		
0	0.1697	0.3998	0.2193
1100	0.1697	0.2704	0.2806
2100	0.1780	0.2302	--
3100	0.1659	0.2326	--
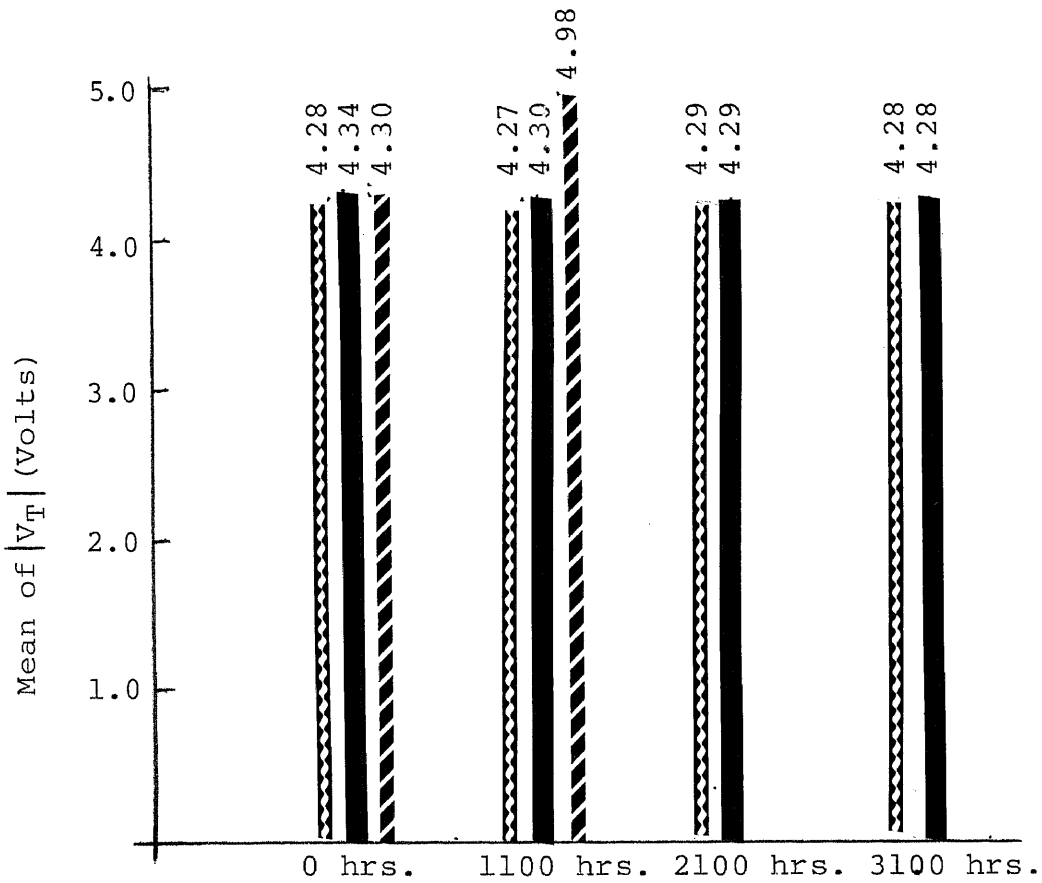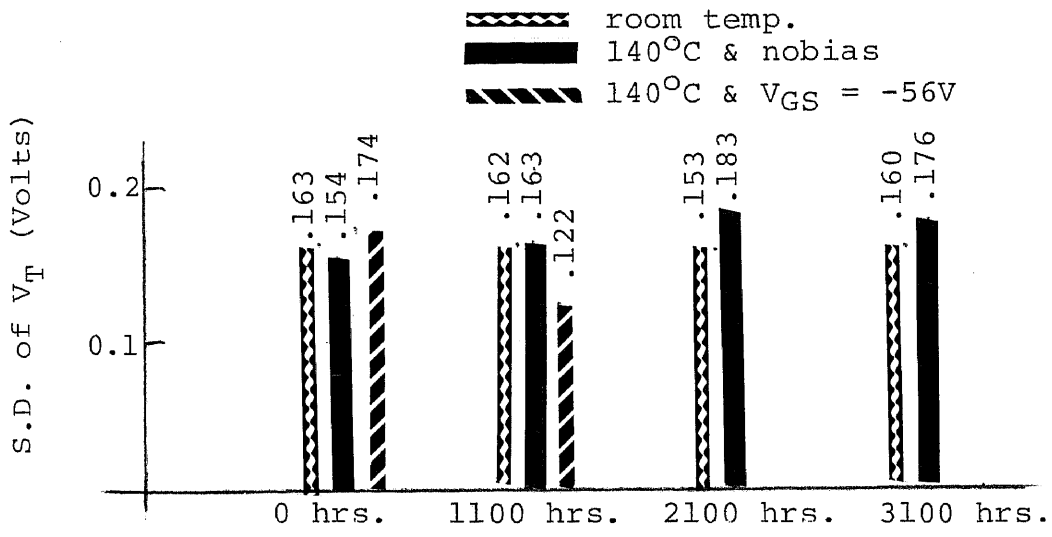
Chart III. Mean & S.D. of V_T – AMI DD08P MOSFET's

room temp.
$140^{\circ}C$ & no bias
$140^{\circ}C$ & $V_{GS} = -56V$

S.D. of V_T (Volts)

0.4
0.3
0.2
0.1

.170 .400 .219
.178 .270 .281
.180 .230
.166 .233

0 hrs.   1100 hrs. 2100 hrs. 3100 hrs.

Mean of $|V_T|$ (Volts)

5.0
4.0
3.0
2.0
1.0

4.34 4.49 4.40
4.30 4.36 5.22
4.34 4.27
4.35 4.25

0 hrs.   1100 hrs. 2100 hrs. 3100 hrs.
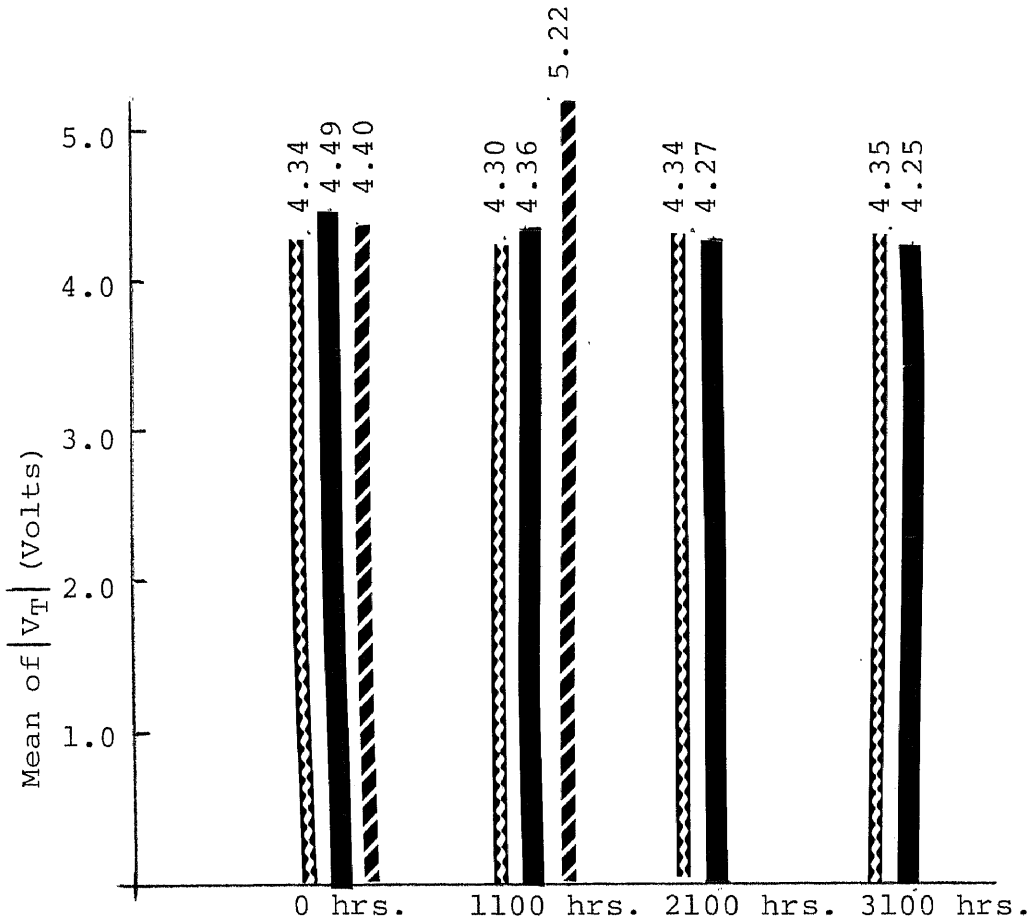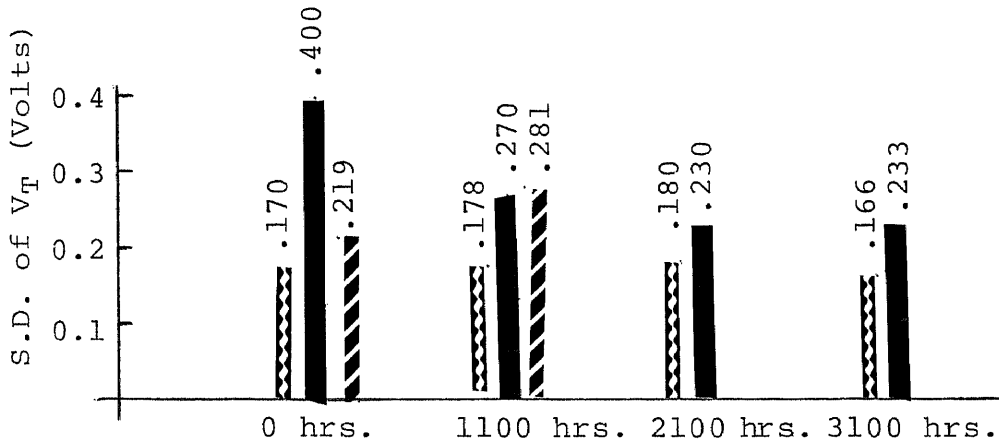
Chart IV. Mean & S.D. of V_T — AMI DD08K MOSFET's

data on the effect of positive and negative gate

bias will be useful. Hence 47 more devices of the

DD08K type were life-tested under the following

new conditions:

Category	Storage Conditions	# of Devices
IIIa	Temperature of $140^{\circ} \pm 5^{\circ}C$ and $V_{GS} = -28V$; source, drain, and substrate tied together	23
IIIb	Temperature of $140^{\circ} \pm 5^{\circ}C$ and $V_{GS} = +28V$; source, drain, and substrate tied together	24

Gate bias of 28V was 40% of the maximum rating,

contributing an electric field in the gate oxide

of about 2.15×10^6 v/cm.

The data obtained on these devices upto 260

hours is summarized in table III. All the IIIb

units (with positive bias) showed an increased $|V_T|$

within 260 hours, the increase in mean $|V_T|$ being 8.7%.

But, out of the 23 IIIa units (with negative bias),

13 showed an average increase in $|V_T|$ of 7.7%, while

the other 10 showed an average decrease of 4.5%.

If all the IIIa units are taken together, mean $|V_T|$

showed an increase of 2.3%. Histograms on

TABLE III

DATA SUMMARY OF HIGH TEMPERATURE POSITIVE AND NEGATIVE

BIAS TESTS ON DD08K MOSFETS:

Mean and Standard Deviation of $|V_T|$

Category	IIIa (140^OC & V_{GS} = -28V)		IIIb (140^OC & V_{GS} = +28V)	
Hours	0	260	0	260
Mean	4.3654	4.4670	4.5265	4.9211
Standard Deviation	0.3996	0.5303	0.3904	0.4355

the percentage drift in $|V_T|$ of these devices
are presented in figures 7 and 8.

11 of the IIIa units were continued on test
upto 1,500 hours. The unit which had shown
increase in $|V_T|$ continued to increase upto about
480 hours and then stabilized. But those units which
had shown decrease in $|V_T|$ began later to increase
and eventually stabilized within 1,500 hours.

In order to confirm the validity of the above
results, an additional larger sample of 22 DD08K
type devices were tested under category IIIa
conditions ($140^{\circ}\pm5^{\circ}$C and V_{GS} = -28V). Threshold
voltage measurements were taken this time at more
frequent time intervals (0 hours, 46, 75, 120,
195, 390, 580, 840, 1200, and 1500 hours). Except
for 1 unit, all the rest drifted in $|V_T|$ to a
lower value at 46 hours. But the $|V_T|$ values started
increasing on all units at least within 390 hours,
and continued to increase beyond 390 hours. The
V_T drift eventually stabilized within 1500 hours.
The data summary on these units is presented in Table
IV and Chart V.

The data on all individual units of category
IIIa, IIIb, and the additional IIIa units are pre-

sented in appendix F.
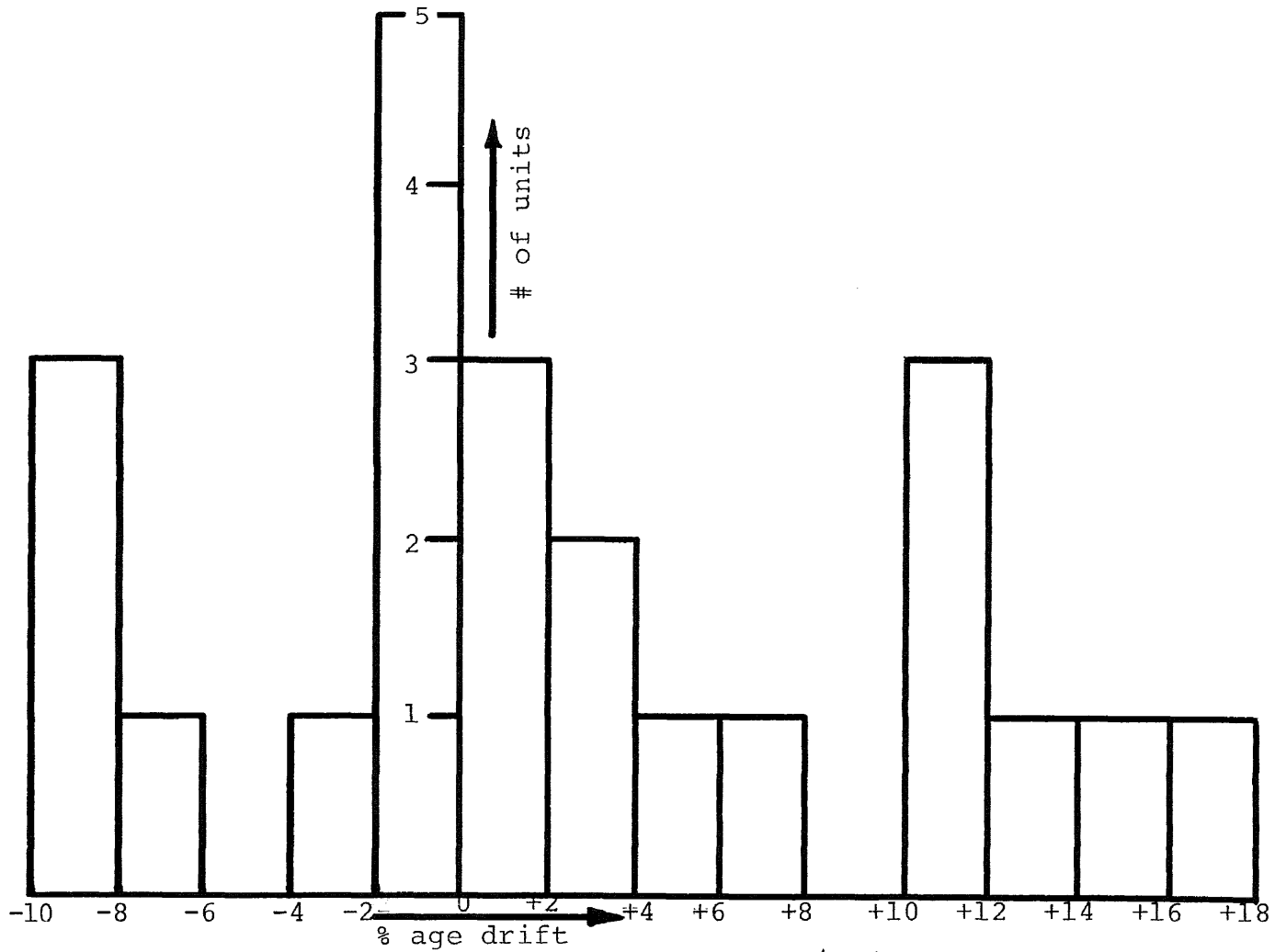
FIG 7. Histogram of % age Drift in $|V_T|$ of III a Units
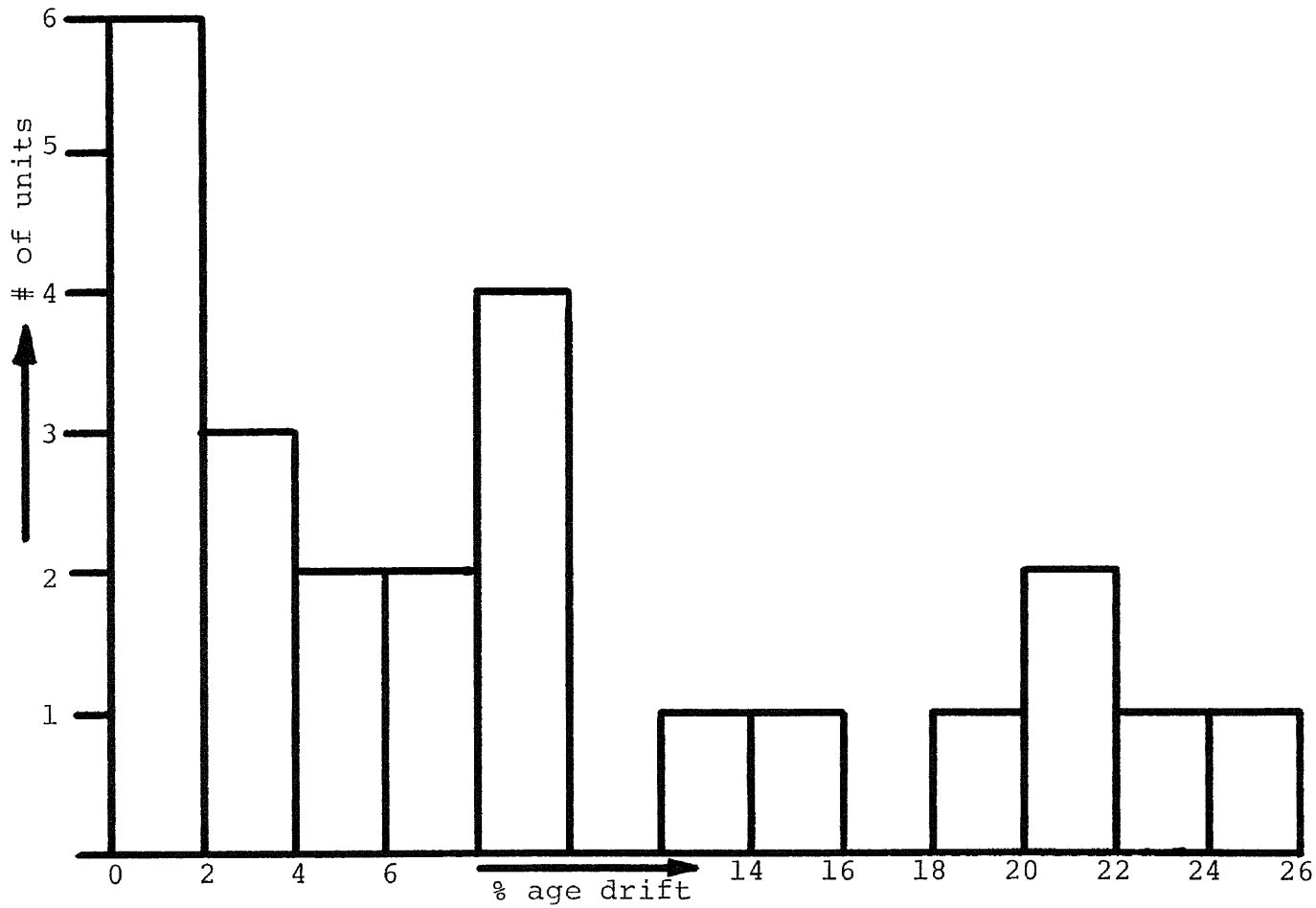
FIG 8. Histrogram of % age Drift in $|V_T|$ of IIIb Units

TABLE IV

DATA SUMMARY OF HIGH TEMPERATURE NEGATIVE BIAS

TESTS ON ADDITIONAL CATEGORY IIIa* MOSFETS

Mean and Standard Deviation of $|V_T|$

HOURS	MEAN	STANDARD DEVIATION
0	4.4458	0.3044
46	4.2826	0.2948
75	4.2279	0.2983
120	4.2014	0.3214
195	4.2343	0.3505
390	4.4283	0.3156
580	4.5436	0.3085
840	4.5994	0.3092
1200	4.6288	0.3091
1500	4.6307	0.3092

* Storage condition: $140^{\circ}C$ and $V_{GS} = -28V$
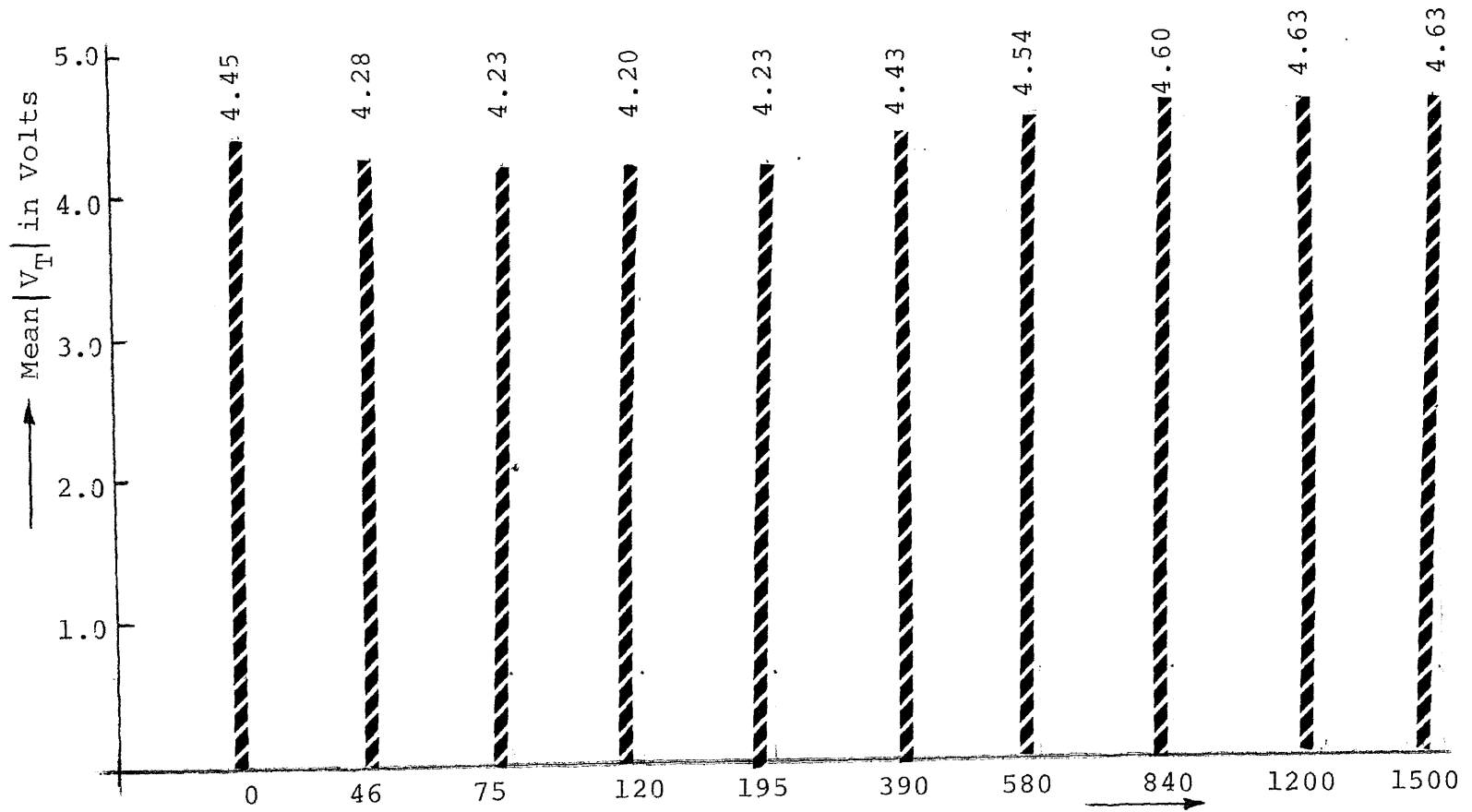
Chart V.   Mean of V_T - Additional DD08K MOSFET's

CHAPTER V

EXPLANATION OF TEST RESULTS AND PROPOSED

THEORY ON THE EFFECT OF NEGATIVE BIAS

5.1. Ionic Contamination of the Oxide:

As has often been reported[96,97,98], the gate

oxide layer of a MOSFET has extraneous ionic

impurities, which have been mostly stated to be

those of alkali metals. Sodium can easily get

introduced into the oxide during the manufacturing

process at any process step. Any process material,

solvent or the ambient can act as a source of sodium.

In addition, hydrogen atoms, when ionized, are

electropositive in nature. Under high enough

electric fields, not only ionization, but also

migration of these ions takes place[100,101]. This

migration however is at a slow rate, and is depend-

ant on temperature as well as size, weight, and

binding energy of the particular ionic impurity

involved. While the hydrogen ions are mobile even

at room temperature, the sodium ions drift occurs at

above 100°C or lower[102]. Some negative charges

have been also noted under certain conditions,

but they do not drift at temperatures much below

300°C, as observed by Deal[102].

The results of life tests presented in chapter
IV show that, while high temperature alone do not
cause the threshold voltage to drift very much,
high temperature along with positive or negative
gate bias cause considerable shifts in V_T.

5.2. Effects of Positive Gate Bias and Temperature:

Under positive gate bias and elevated
temperature, the elctropositive impurity ions in
the gate oxide tend to migrate towards the oxide-
silicon interface, as shown in figure 9. The
increased positive ionic charge density near the
oxide-silicon interface tends to oppose channel
inversion (see figure), and hence necessitates a
higher applied negative gate voltage to invert
the channel. In other words, the threshold volt-
age of the device becomes more negative. This
can also be seen directly from the expression for
V_T given in section 2.3., and is consistent with
the test results obtained on category IIIb units
($140^\circ C$ & $V_{GS} = +28V$). Figure 10 shows the condi-
tions under V_T measurements for this case.

5.3. Effects of Negative Gate Bias and Temperature:

Under negative gate bias of $V_{GS} = -56V$ and
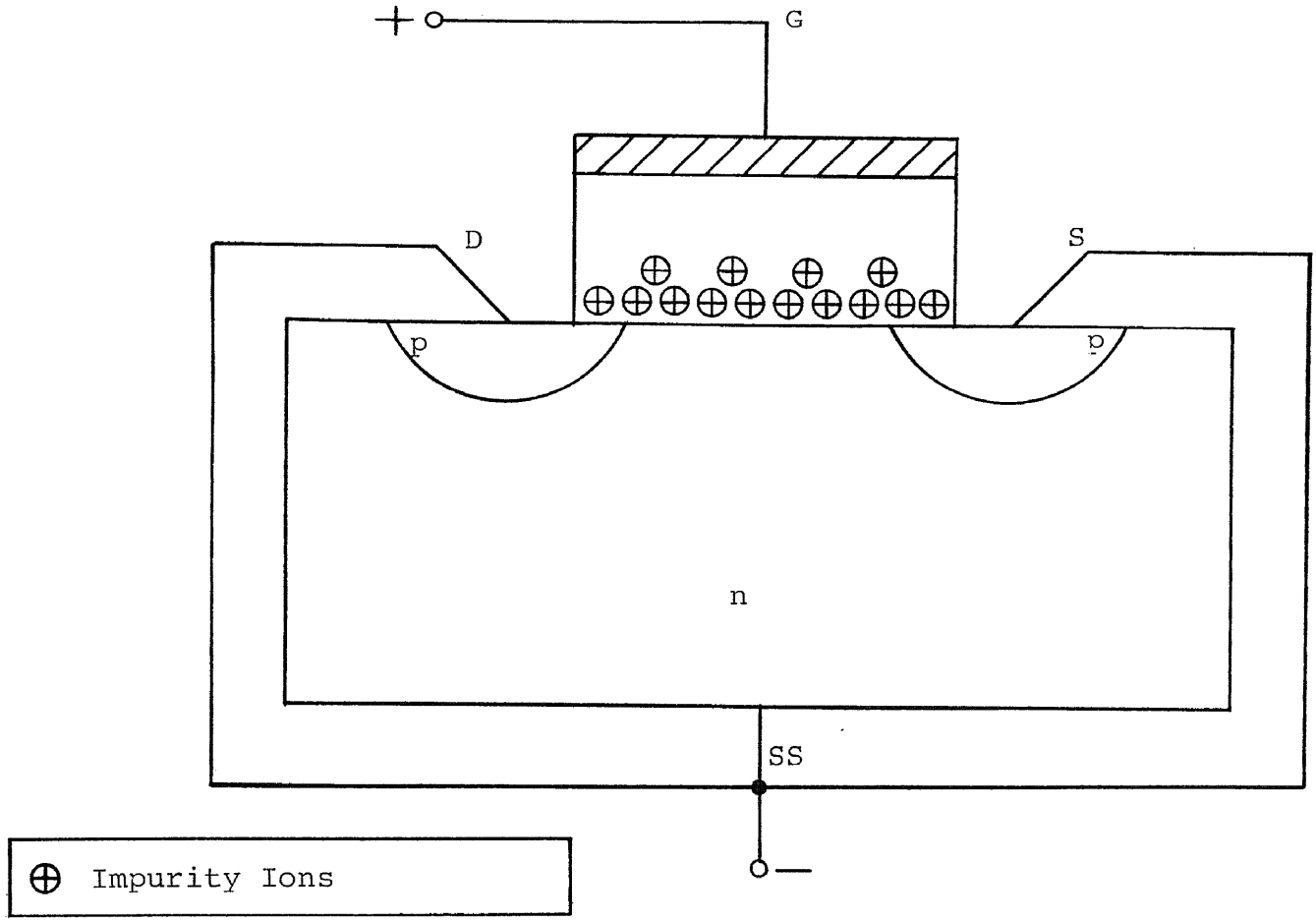
⊕ Impurity Ions

FIG 9. Conditions Under Positive Gate Bias & Temperature
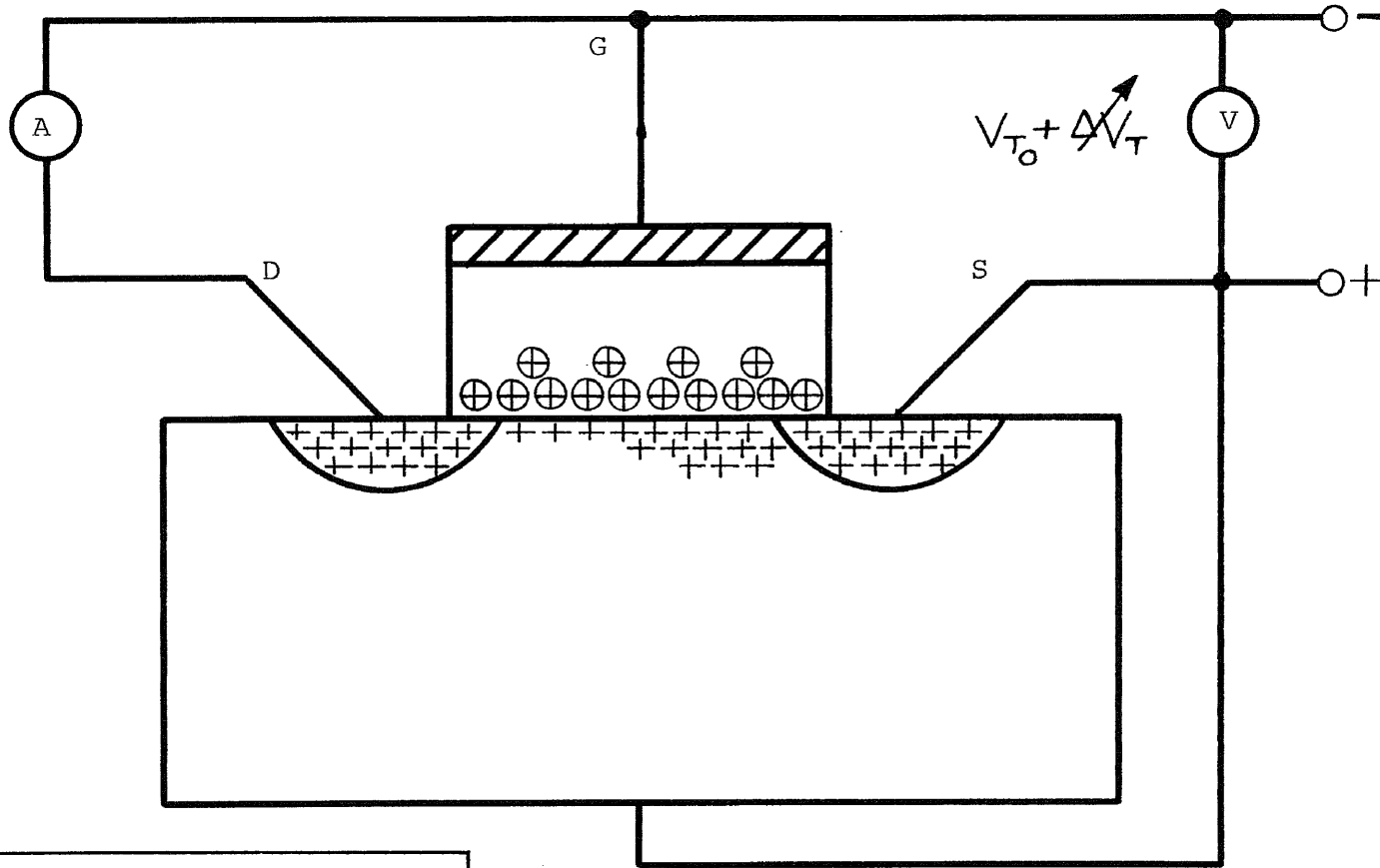
+   Holes

⊕   Impurity Ions

FIG 10.

temperature of 140°C, the threshold voltage

of all the IIc units were found to drift towards

more negative values when the tests were

carried to 1100 hours. But tests at V_{GS} = -28V

and 140°C (IIIa units) revealed V_T drifts in

both directions upto 260 hours, but between

260 hours and the next set of readings taken

at 360 hours, all the units had drifted towards

more negative V_T values. They continued to

do so beyond 360 hours also, and the drift even-

tually stabilized within 1200 hours. The same

pattern of drift was exhibited by the additional

IIIa units also.

A survey of the literature revealed that

the papers of Deal et al[103], Hofstein[104], Reynolds

et al[105], and Kim[106] are relevant to the phenomena

observed, though none of them bring out explicitly

the theoretical factors causing the observed thres-

hold voltage shifts. But taking the contents of

these four papers together and the experimental

results of this investigation, the occurence of

the following two competing mechanisms is herein

postulated:

    1. <u>Impurity ion migration</u>: Under negative gate

bias, the electropositive impurity ions tend
to migrate towards the metal-oxide interface.
The consequent decrease in the positive ionic
charge density near the oxide-silicon inter-
face helps channel inversion, and hence
only a lower applied negative gate voltage is
required for channel inversion, or $|V_T|$ tends
to decrease. This can also be seen from the
expression for V_T given in section 2.3. This
migration phenomenon should saturate, if the
bias stress is continued for sufficient
length of time, once all the available impurity
ions have migrated to the metal-oxide inter-
face.

2. Augmentation of positive charge density at the
   oxide-silicon interface: Since the thermal
   oxidation process itself takes place by the
   inward diffusion of oxygen through the silicon
   dioxide already formed in the outer layers, it
   is inevitable that the last two hundred ang-
   stroms or so of the oxide layer near the oxide-
   silicon interface are only partially oxidized,
   leaving some SiO atoms and some unoxidized Si
   atoms. If a high enough negative field at
   elevated temperature is applied across
   the oxide, these unoxidized Si atoms are

positively ionized. The silicon in the partially

oxidized zone could also be considered as

providing traps for holes. A high enough negative

gate bias at high temperature can also attract

into the oxide layer more positively ionized Si

from the substrate regions near the interface. The

net effect of all these is to cause an increase

in the positive ionic charge density at the oxide-

semiconductor interface. Such an augmentation of

positive charge density at the oxide-silicon inter-

face tends to oppose channel inversion. In other

words, $|V_T|$ will tend to increase.

Figures 11 and 12 depict the combined picture of the

conditions under negative gate bias and temperature,

and the conditions under V_T measurement respectively.

Considering the ion migration mechanism, Marciniak

and Przewlocki[107] obtained drift time constants for

positive bias and temperature one or two orders of

magnitude higher than those for the opposite polarity,

and attributed their results to a possible trapping of

mobile ions at the metal-oxide interface. If this

theory is valid, it would follow that the increase in

$|V_T|$ due to ion migration in the negative bias case would

be less in magnitude and saturate faster, than in the

case of positive bias. This is consistent with the

Conditions Under Negative Gate Bias & Temp.

Impurity Ions

Silicon Ions

FIG 11.
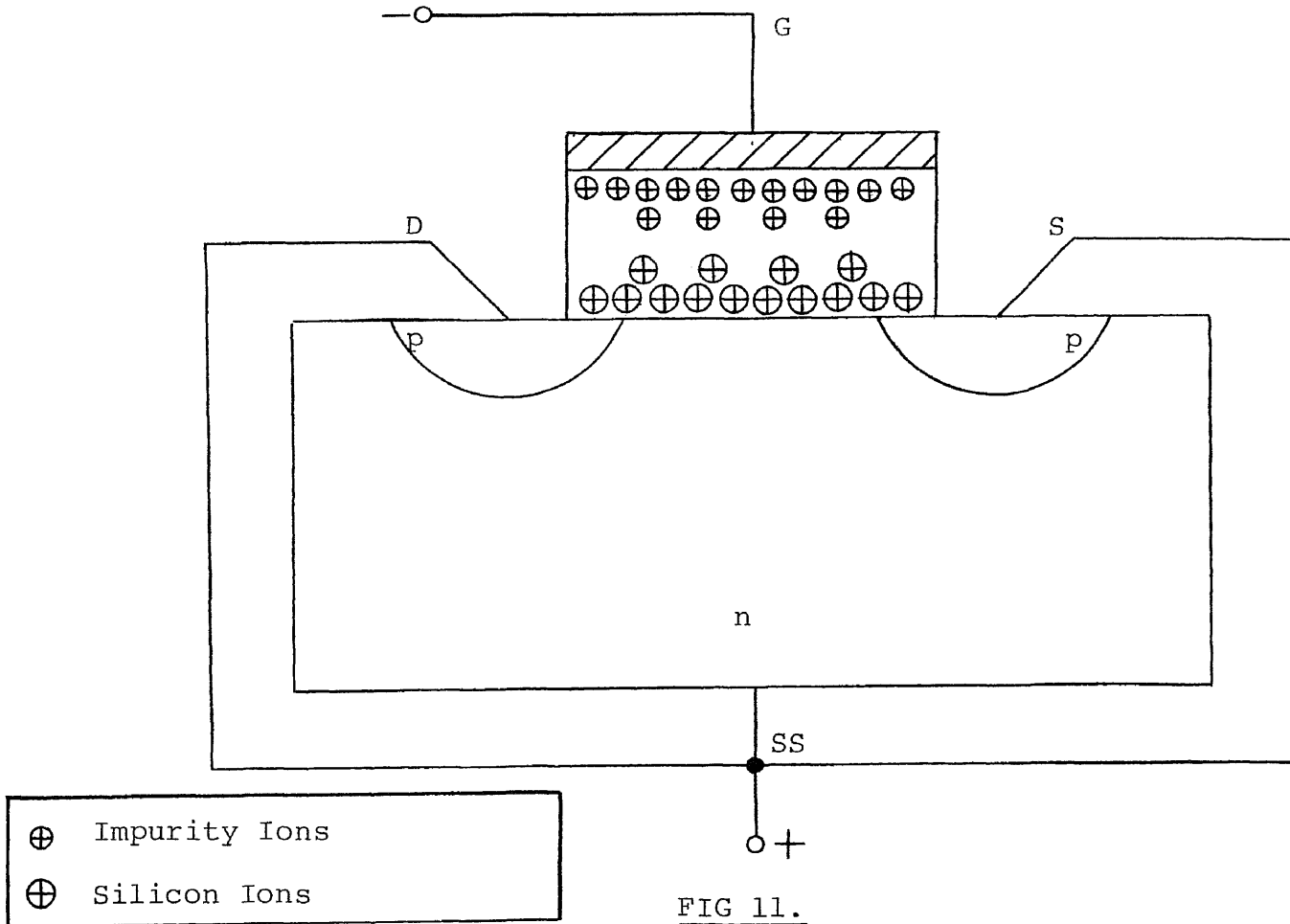
Conditions at V_T Measurement (-ve Gate Bias & Temp.)

$V_{T_0} \pm \Delta V_T$

G

D

S

SS

⊕ Impurity Ions

+ Holes
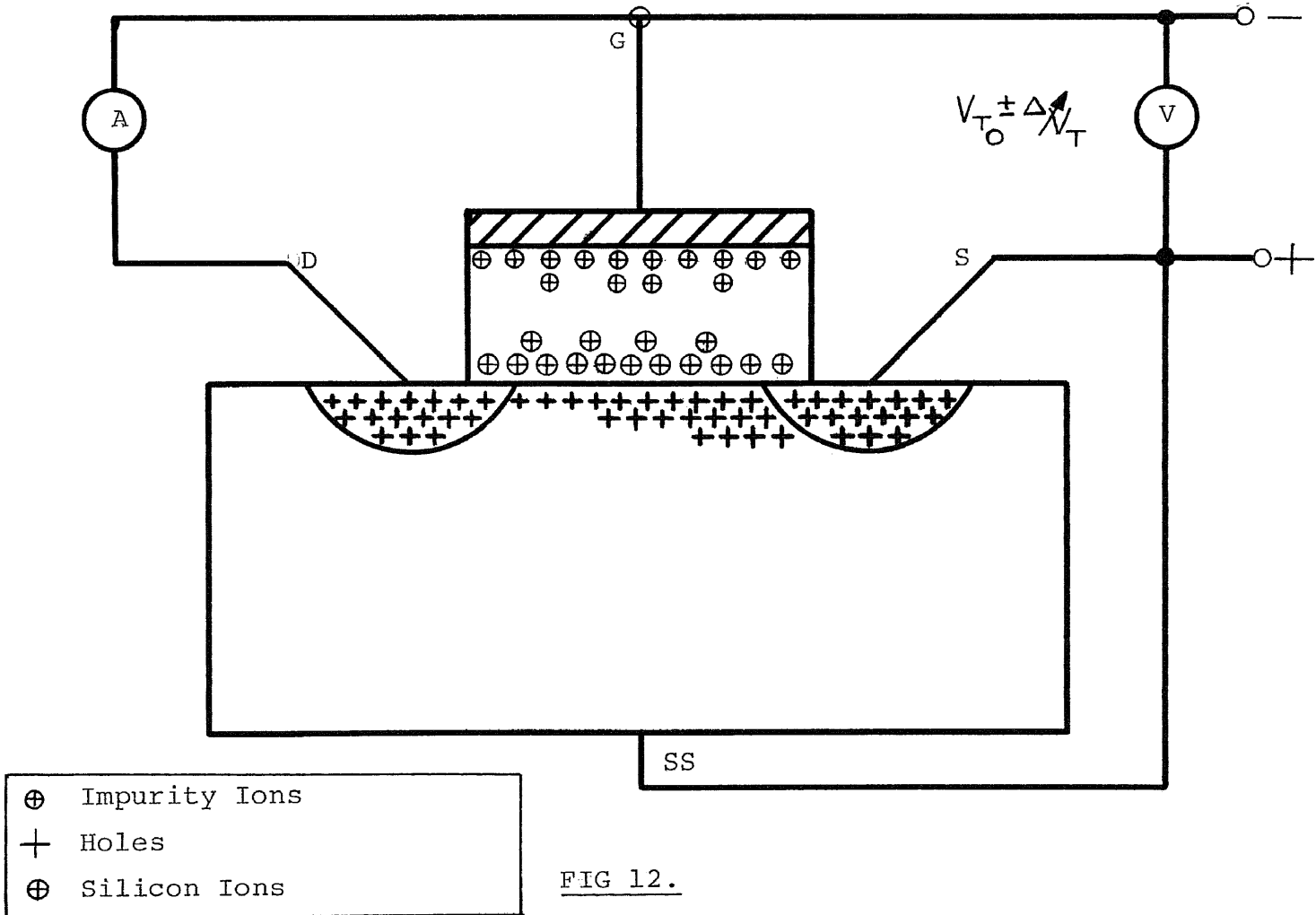
⊕ Silicon Ions

FIG 12.

results obtained on the 260 hours test of category
IIIa and IIIb units.

Considering the latter mechanism, the presence of
the unoxidized silicon is believed also to be the
cause of Q_{SS}[108]. Under negative bias, the positive
charging of the unoxidized silicon increases the
threshold voltage magnitude. Deal[109] found that
at $300^\circ C$, the drift with time reached 90 percent of
the saturation value within 10 minutes and the
remaining 10 percent took 8 hours, when the applied
field was between 0.5×10^6 to 3.0×10^{-6} V/cm. At
the $140^\circ C$ temperature and 2.3×10^{-6} V/cm field used
in the tests of this study, this period can be expected
to be much longer.

The period required for the saturation of the
drift due to the second mechanism is much longer than
that required for the stabilization of the drift due
to the first mechanism. Thus, when the test duration
is small, either of the two competing mechanisms could
dominate; while for longer test duration, the second
effect becomes dominant at least after a few tens or
hundreds of hours. Thus, the threshold voltage drifts
eventually towards more negative values. The postulation
set forth is thus consistent with the test results

presented in chapter IV.

CHAPTER VI

CONCLUSIONS AND RECOMMENDATIONS

6.1. Conclusions:

P-channel MOSFET's under negative gate bias
and temperature stress may often show a downward
drift in $|V_T|$ initially, meaning a few tens to
a few hundreds of hours, depending on the field,
temperature, and impurity concentration. But
after this period, the drift in $|V_T|$ is upward.
The reason for this is that the migration of
impurity ions in the oxide layer predominates
initially over the positive ion augmentation
effect, while as time progresses, the latter
has the dominant effect.

For the positive gate bias and temperature
stress however, the drift in $|V_T|$ is upward through-
out.

6.2. Recommendations:

During the manufacturing process, contamina-
tion by ionic impurities should be eliminated or
reduced to a minimum. Advances have been made
by the industry in this direction, but sustaining
the necessary process controls can not be over-

emphasized.

Further studies are required to determine what part of the augmentation of positive charge density at the silicon-silicon dioxide interface is due to the infusion of additional silicon ions into the oxide from the substrate, and what part is due to additional charging of ionized silicon responsible for Q_{ss}.

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SCREEN	CLASS B		
	MIL-STD-883 METHOD	CONDITION	REQUIREMENT (%)
3.1.1 INTERNAL VISUAL (PRECAP)	2010	TEST CONDITION B	100
3.1.2 STABILIZATION BAKE	1008	24 HRS MIN TEST CONDITION C MIN	100
3.1.3 THERMAL SHOCK	1011	-	-
3.1.4 TEMPERATURE CYCLING	1010	TEST CONDITION C MIN.	100
3.1.5 MECHANICAL SHOCK	2002	-	-
3.1.6 CONSTANT ACCELERATION	2001	TEST CONDITION E (MIN) Y_1 PLANE	100
3.1.7 HERMETICITY a. FINE b. GROSS	1014	-	100
3.1.8 INTERIM (PRE-BURN-IN) ELECTRICAL PARAMETERS	PER APPLIC-ABLE PROCURE-MENT DOCUMENT	-	PER APPLICABLE DOCUMENT
3.1.9 BURN-IN TEST	1015	160 HOURS AT 125°C MIN.	100

SCREEN	CLASS B		
	MIL-STD-883 METHOD	CONDITION	REQUIREMENT (%)
3.1.10 INTERIM (POST-BURN-IN) ELECTRICAL PARAMETERS	PER APPLICABLE PROCUREMENT DOCUMENT	-	-
3.1.11 REVERSE-BIAS BURN-IN	1015	TEST CONDITION A OR C, WHEN SPECIFIED 72 HRS. AT 150°C MIN.	-
3.1.12 FINAL ELECTRICAL TEST a. STATIC TESTS 1. 25°C 2. MAX AND MIN RATED OPERATING TEMPERATURE b. DYNAMIC TESTS 25°C	PER APPLICABLE PROCUREMENT DOCUMENT	-	100
3.1.13 RADIOGRAPHIC	-	-	-
3.1.14 QUALIFICATION OR QUALITY CONFORMANCE INSPECTION TEST SAMPLE SELECTION	5005	-	PER APPLICABLE DOCUMENT
3.1.15 EXTERNAL VISUAL	2009	-	100

APPENDIX B.

FAILURE MODES OF MOS DEVICES

1. Defects due to electrical overstress:

    1.1. Open bond wires
    1.2. Punctured gate oxide
    1.3. Blown protective devices

2. Oxide faults:

    2.1. Pinholes
    2.2. Cracks
    2.3. Contamination

3. Metallization faults:

    3.1. Lifting metal
    3.2. Over-alloying
    3.3. Cracks in metal
    3.4   Too thin metal
    3.5. Bridging metal
    3.6. Corroded metal

4. Surface defects:

    4.1. Contamination, ionic and particulate
    4.2. Excessive accumulation or depletion
    4.3. Inversion or channeling

5. Die-mount faults:

    5.1. Misplaced die
    5.2. Poor adhesion and voids under die
    5.3. Eutectic on die

6. Wire-bonding faults:

    6.1. Broken wire
    6.2. Mis-targeted bonds
    6.3. Improper ball size
    6.4. Excessive wire tails
    6.5. Excessive slackness
    6.6. Crossing of wires
    6.7. Poor bond-pull strength
    6.8. Purple plague

7. Package defects:

    7.1. Poor hermeticity
    7.2. Mechanical damage
    7.3. Poor lead integrity
    7.4. Contamination due to weld splash and
          improper cleaning

8. Diffusion faults

APPENDIX C

RECOMMENDED SEQUENCE OF INDIVIDUAL STEPS FOR FAILURE
ANALYSIS**

1. External visual examination.
2. Electrical tests (through package pins only) for verification.
3. X-ray.
4. Hermetic seal test (fine).
5. Hermetic seal test (gross).
6. Ultra-violet inspection.
7. Gas sample (of package cavity).
8. Decapsulation.
9. Die photo.
10. Visual inspection.
11. SEM inspection.
12. Thermal profile.
13. Electrical probing.
14. Wire-pull tests.
15. Passivation oxide removal.
16. Probing-electrical tester.
17. Selective removal of metal.
18. Decoration technique.
19. Etching SiO_2.
20. Bevel/stain.
21. Diffusion profile by spreading resistance measurement.
22. Sirtl etch.
23. Cross-section.
24. Store sample.
25. Record data.

_____

** Basic Technology by Integrated Circuit Engineering,
   Scottsdale, Arizona, pp. 21-14/15.

A P P E N D I X   D

SUMMARY OF BASIC FAILURE ANALYSIS TECHNIQUES ***

METHOD	PRINCIPLE	PHENOMENON	ADVANTAGES	LIMITATIONS
Infrared Spectroscopy	Structure determination and identity of organic and inorganic compounds. General quant. analysis.	Excitation of molecular vibrations by light.	Identification of functional groups. Virtually no sample limitations. Impurity detection.	Medium sensitivity. No direct information about size of molecule.
Mass Spectrometry	Structure Determination and identity of organic compounds. Analysis of trace volatiles in non-volatiles.	Ionization of molecule and cracking of molecule into fragment ions.	Precision molecular wt.(molecular ion). Very high sensitivity. Impurity detection.	Does not detect functional groups directly. Comparitively slow & destructive.
Gas Chromatography	General multi-component quantative analysis of volatile organics. Highly efficient separation technique.	Partitioning between vapor phase and substrate.	Generality-- Widely applicable to volatile materials. Multi-component analysis. High sensitivity in special cases.	Identifies materials only in special cases. Not applicable to materials of low volatility.

METHOD	PRINCIPLE	PHENOMENON	ADVANTAGES	LIMITATIONS
Combined Gas Chromatography and Mass Spectrometry.	Identification and analysis of trace organic materials.	Combines separation efficiency of GC with sensitivity and specificity of mass spectroscopy.	Applicable to identity of sub-ppm components in mixtures.	Not applicable to materials of low volatility.
Atomic Emission Spectroscopy (AES)	General qual. and semiquant. survey of all metallic elements. Trace metal analysis.	Light emission from excited electronic states of atoms.	General for all metallic elements. Simultaneous analysis of all metallic elements.	Detects the volatile elements (non-metals) only with difficulty; calibration required for precision quant analysis.
Radiographic X-ray	Detect loose particles in hermetic packages.	X-rays penetrate into cavity. Metallic particles are opaque to X-rays.	Loose metallic particles may-be detected without disturbing seal in easy, non-destructive manner.	Metal packages shield circuits from X-rays. Electrically programmable ROM's will be damaged.

METHOD	PRINCIPLE	PHENOMENON	ADVANTAGES	LIMITATIONS
Leak Test	Determine hermiticity of packages.	Fine leak tests force detectable material in package and detects its escape.	Eliminates possible field failures and determines possible cause of failed devices.	Correlation between leak rate and failure rate not documented.
Spreading Resistance	Measures resistivity.	Resistance between two probes is function of proble characteristics, resistivity & geometry of material	High spatial resolution can be obtained.	Calibration of probe characteristics and proper surface preparation of chip is essential.
Plasma Etching	Remove glassivation. Also used to remove silicon.	Ionized fluorine etch attacks SiO_2 and Si & not aluminum	Removes glassivation without damaging aluminum metallization or adding other contaminants.	Requires additional equipment.

METHOD	PRINCIPLE	PHENOMENON	ADVANTAGE	LIMITATIONS
Electron Micro-Probe (EMP)	Identifies specific elements and to some degree the concentration.	High energy electron beam causes electrons to be ejected from bombarded material. Emitted X-ray photon energy identifies element.	High resolution and simultaneous display of all elements	Equipment costs.
Flying Spot Scanner	Troubleshoot defective circuits.	Generation of hole-electron pairs by light beam in junction areas.	Non-destructive low energy light beam used.	Metallization shields light. Technique not well developed.
Infrared Scanning	Determine thermal profile.	Detect infrared radiation from scanned chip.	Non-destructive convenient method of detecting hot spots.	Resolution inadequate for small geometries of high frequency circuits.

APPENDIX E

SPECIFICATIONS OF AMI DD07P, DD07K, DD08P, AND DD08K MOSFETs

General Description: Medium Conductance P-channel

Enhancement Mode MOSFET's in

TO-72 Package.

Terminal Diagrams - Bottom View

DD07P / DD07K   DD08P / DD08K

(Gate Protected)   (Not gate protected)
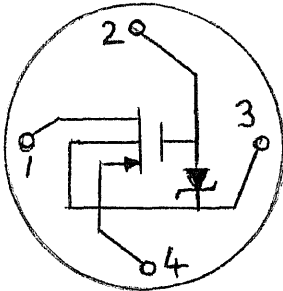
1. Drain
2. Gate
3. Body
4. Source
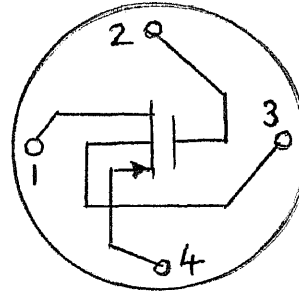
Absolute Maximum Ratings $(T_A = 25^O C$, Body Grounded)

		DD07P/K	DD08P/K
V_{DSS}	Drain-to-Source Voltage	-30V	-30V
V_{SDS}	Source-to-Drain Voltage	-30V	-30V
V_{GD}	Gate-to-Source Voltage	-30 to +0.3V	±70V
V_{GS}	Gate-to-Source Voltage	-30 to +0.3V	±70V
V_{DB}	Drain-to-Body Voltage	-30 to +0.3V	-30 to +0.3V
V_{SB}	Source-to-Body Voltage	-30 to +0.3V	-30 to +0.3V
V_{GB}	Gate-to-Body Voltage	-30 to +0.3V	±70V
I_{DS}	Drain-to-Source Current	50 mA	50 mA

SYMBOL	CHARACTERISTICS	MIN.	TYP.	MAX.	UNITS	TEST CONDITIONS
V_T	Threshold Voltage	-3.5	-4.3	5.5	V	$V_{GS} = V_{DS}$, $I_{DS} = -10$ uA
BV_{DSS}	Drain-Source Breakdown	-30	-41	-	V	$I_{DS} = -10$ uA, $V_{GS} = 0$
BV_{SDS}	Source-Drain Breakdown	-30	-41	-	V	$I_{SD} = -10$uA, $V_{GD} = 0$
BV_{PNG}	Body Breakdown	-30	-41	-	V	$I_{DB} = -10$uA, $V_{GS} = 0$, Source Open
BV_{GSS}*	Gate-Source Breakdown	-30	-41	-	V	$I_{GS} = -10$uA, $V_{DS} = 0$
I_{DSS}	Drain Leakage	-	0.05	1.0	nA	$V_{DS} = -15$V, $V_{GS} = 0$
I_{SDS}	Source Leakage	-	0.07	1.0	nA	$V_{SD} = 15$V, $V_{GD} = 0$
I_{GSS}*	Gate Leakage	-	0.01	1.0	nA	$V_{GS} = -15$V, $V_{DS} = 0$
I_{GSS}	Gate Leakage	-	0.1	-	pA	$V_{GS} = -30$V, $V_{DS} = 0$
I_{DSon}	ON Drain Current	15.5	44.0	-	mA	$V_{GS} = V_{DS} = -15$V
R_{ON}	DC ON Resistance	-	125	200	ohms	$V_{GS} = -15$V, $V_{DS} = -0.10$V
Y_{fs}	Forward Transadmittance	4000	5400	-	umho	$V_{GS} = -15$V, $V_{DS} = -15$V, F = 1.0 kHz
r_d	Dynamic Drain Resistance	-	2.0	-	kohm	$V_{GS} = -15$V, $V_{DS} = -15$V, F = 1.0 kHz
C_{iss}	Input Capacitance	-	4.4	6.0	pF	$V_{GS} = 0$, $V_{DS} = 0$
C_{oss}	Output Capacitance	-	4.6	6.0	pF	$V_{GS} = 0$, $V_{DS} = 0$

SYMBOL	CHARACTERISTICS	MIN.	TYP.	MAX.	UNITS	TEST CONDITIONS
C_{rss}	Reverse Transfer Capacitance	–	0.60	1.00	pF	$V_{GS} = 0$, $V_{DS} = 0$, $C_{rss} = C_{gd}$
C_{gs}	Gate-to-Source Capacitance	–	3.8	5.0	pF	$V_{GS} = 0$, $V_{DS} = 0$
C_{ds}	Drain-to-Source Capacitance	–	4.0	5.0	pF	$V_{GS} = 0$, $V_{DS} = 0$
F_i	Input Gain Bandwidth Frequency	–	195	–	MHz	$F_i = Y_{fs}/2\pi\, C_{iss}$
F_o	Output Gain Bandwidth Frequency	–	187	–	MHz	$F_o = Y_{fs}/2\pi\, C_{oss}$

* With gate protective zener (DD07P, DD07K)

A P P E N D I X   F

TEST DATA ON ALL INDIVIDUAL DEVICES

V_T OF CATEGORY IIIa MOSFETs

(Units Stored at 140^OC & With a Bias of V_{GS} = -28V)

Unit No.	V_T at 0 hrs.	V_T at 260 hrs.	Percentage Drift in V_T
N1	3.9796	4.4533	+ 11.90
N2	4.8175	5.6749	+ 17.80
N3	4.0085	3.9309	− 1.84
N4	4.9755	4.6118	− 7.31
N5	4.4798	4.9827	+ 11.23
N6	4.5138	5.1503	+ 14.10
N7	3.8823	4.0100	+ 3.29
N8	4.6708	4.9116	+ 5.16
N9	4.8095	4.3564	− 9.42
N10	4.0738	4.0384	− 0.87
N11	4.6679	4.6147	− 1.14
N12	3.9880	3.9133	− 1.87
N13	4.0443	4.1057	+ 1.52
N14	4.0000	4.0313	+ 0.78
N15	4.1900	4.0847	− 2.51
N16	4.0239	4.2912	+ 6.64
N17	4.8779	4.3911	− 9.98
N18	4.1027	4.0469	− 1.36
N19	3.9321	3.9621	+ 0.76
N20	4.4232	4.5502	+ 2.87

V_T OF CATEGORY IIIa MOSFETS - continued

Unit No.	V_T at 0 hrs.	V_T at 260 hrs.	Percentage Drift in V_T
N21	5.2145	5.9066	+ 13.27
N22	4.7600	4.3421	- 8.78
N23	3.9721	4.3820	+ 10.32

Mean   =   4.3654   4.4670

S.D.   =   0.3996   0.5303

V_T OF CATEGORY IIIb MOSFETs

(Units Stored at 140°C & With a Bias of V_{GS} = +28V)

Unit No.	V_T at 0 hrs.	V_T at 260 hrs.	Percentage Drift in V_T
P1	4.5584	4.6315	+ 1.60
P2	4.5418	4.6088	+ 1.48
P3	4.3365	4.4480	+ 2.57
P4	4.7370	4.9654	+ 4.82
P5	4.2429	4.6343	+ 9.22
P6	4.0394	4.4320	+ 9.72
P7	4.9050	5.2248	+ 6.52
P8	4.5343	4.8756	+ 7.53
P9	4.9527	4.9667	+ 0.28
P10	5.0017	5.0561	+ 1.09
P11	5.0861	6.2191	+ 22.28
P12	3.7540	4.7158	+ 25.62
P13	4.4996	4.6408	+ 3.14
P14	4.1640	4.3598	+ 4.70
P15	4.2916	4.6743	+ 8.92
P16	4.6090	5.5628	+ 20.69
P17	4.0149	4.7885	+ 19.27
P18	4.8065	4.8671	+ 1.26

V_T OF CATEGORY IIIb MOSFETs - continued

Unit No.	V_T at 0 hrs.	V_T at 260 hrs.	Percentage Drift in V_T
P19	4.9717	5.0653	+ 1.88
P20	4.4900	5.1895	+ 15.58
P21	5.1204	5.3088	+ 3.68
P22	4.9340	5.5596	+ 12.68
P23	4.1582	5.0465	+ 21.36
P24	3.8870	4.2664	+ 9.76

Mean   =   4.5265   4.9211

S.D.   =   0.3904   0.4355

V_T OF CATEGORY IIIa MOSFET's CONTINUED ON TEST

(Units Stored at 140^OC & $V_{GS} = -28$V)

Unit #	0 hrs.	260 hrs.	360 hrs.	480 hrs.	910 hrs.	1500 hrs.
N13	4.0443	4.1057	4.1963	4.2000	4.2004	4.2002
N14	4.0000	4.0313	4.1603	4.2769	4.2807	4.2810
N15	4.1900	4.0847	4.1735	4.2668	4.2683	4.2688
N16	4.0239	4.2912	4.3700	4.4311	4.4517	4.4529
N17	4.8779	4.3911	4.6263	4.6590	4.6630	4.6653
N18	4.1027	4.0469	4.1123	4.1980	4.2008	4.2010
N19	3.9321	3.9621	4.0612	4.0872	4.0896	4.0891
N20	4.4232	4.5502	4.6555	4.6992	4.7032	4.7003
N21	5.2145	5.9066	6.0960	6.1970	6.2401	6.2398
N22	4.7600	4.3421	4.4034	4.4712	4.6010	4.6853
N23	3.9721	4.3820	4.5075	4.6179	4.6289	4.6304

V_T OF ADDITIONAL UNITS OF CATEGORY IIIa

(Units at $140^{O}C$ and $V_{GS} = -28V$)

Unit #	0 hrs.	46 hrs.	75 hrs.	120 hrs.	195 hrs.
N51	4.3275	4.2153	4.1608	4.1137	4.0985
N52	4.7333	4.4720	4.3511	4.3207	4.4601
N53	4.4135	4.2209	4.1212	4.0150	4.2195
N54	4.3584	4.1083	4.0008	3.9000	3.8595
N55	4.7409	4.5612	4.4803	4.4987	4.5593
N56	4.8613	4.7673	4.7287	4.6801	4.6898
N57	4.4860	4.2073	4.0803	3.8795	3.7087
N58	4.6698	4.4682	4.3611	4.2602	4.2085
N59	3.9743	3.7094	3.6712	3.7733	3.8595
N60	4.0935	3.8847	3.7930	3.6373	3.5987
N61	4.4492	4.3360	4.3133	4.3275	4.3623
N62	4.1239	4.0591	4.0400	4.0175	4.0408
N63	4.7775	4.5384	4.5023	4.5187	4.5593
N64	4.1283	4.0393	4.0187	3.9753	3.9806
N65	4.6193	4.3875	4.3213	4.3408	4.4389
N66	4.6920	4.5527	4.5013	4.4727	4.5198
N67	4.7340	4.5605	4.5197	4.5503	4.6010
N68	4.8027	4.5849	4.5423	4.5588	4.6168
N69	4.6280	4.3339	4.2697	4.2716	4.3279
N70	3.9273	3.7361	3.6989	3.7079	3.7593
N71	4.3223	4.5334	4.6000	4.6811	4.7612

^V_T OF ADDITIONAL UNITS OF CATEGORY IIIa - continued

Unit #	0 hrs.	46 hrs.	75 hrs.	120 hrs.	195 hrs.
N72	3.9455	3.9412	3.9387	3.9312	3.9254

Unit #	390 hrs.	580 hrs.	840 hrs.	1200 hrs.	1500 hrs.
N51	4.3004	4.4419	4.5087	4.5133	4.5129
N52	4.7993	4.9404	4.9998	5.0007	5.0013
N53	4.4802	4.5614	4.5996	4.6012	4.6103
N54	4.2734	4.4883	4.5553	4.5996	4.5987
N55	4.7112	4.7914	4.8189	4.8205	4.8216
N56	4.8014	4.8773	4.8823	4.8847	4.8883
N57	4.3388	4.5197	4.5604	4.6024	4.6042
N58	4.3987	4.6411	4.7887	4.8491	4.8508
N59	3.9937	4.0488	4.0850	4.1089	4.1074
N60	3.9001	4.1111	4.1889	4.2302	4.2299
N61	4.4558	4.5094	4.5313	4.5507	4.5523
N62	4.1611	4.2285	4.2638	4.2893	4.2966
N63	4.6815	4.8009	4.8933	4.9414	4.9474
N64	4.0809	4.1757	4.2418	4.2989	4.3021
N65	4.6197	4.7213	4.8076	4.8683	4.8702
N66	4.6887	4.8011	4.8635	4.9011	4.9013
N67	4.7203	4.7997	4.8384	4.8607	4.8599
N68	4.7649	4.8410	4.8808	4.9089	4.9072

V_T OF ADDITIONAL UNITS OF CATEGORY IIIa - continued

Unit #	390 hrs.	580 hrs.	840 hrs.	1200 hrs.	1500 hrs.
N69	4.5125	4.6844	4.7904	4.8583	4.8603
N70	3.9001	4.0012	4.0778	4.1192	4.1201
N71	4.8487	4.8985	4.9123	4.9272	4.9303
N72	3.9902	4.0753	4.0987	4.0998	4.1012

APPENDIX G

THRESHOLD VOLTAGE DEFINITIONS

The definitions and expressions for V_T, given in chapter II, are based on the assumption that conduction is deemed to have commenced, when the channel surface has become as much p in nature as the bulk is n. In section 2.2, V_T is hence defined as the gate voltage required to produce sufficient Q_G to counteract the surface state charge Q_{SS} and the charge Q_D of a depletion region that supports a potential of $2\emptyset_F$. In figure 2, the same definition is expressed in terms of charge distributions as below:

$$- Q_G = Q_{SS} + Q_D + Q_I$$

In the expression for V_T given in section 2.3, the term Q_B (charge density in the bulk silicon) is equal to $(Q_D + Q_I)$, the total hole charge in the depletion region and the inverted channel, due to the applied gate voltage. This expression also includes terms to take into account the effects of (i) the work function difference between the gate metal and the silicon and (ii) any ionic contamination in the gate oxide.

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