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CONCEPTS IN LSI SERVO-CONTROL-ELECTRONICS

BY

ALFONS TUSZYNSKI

A DISSERTATION

PRESENTED IN PARTIAL FULTILLMENT OF

THE REQUIREMENTS FOR THE DEGREE

OF

DOCTOR OF ENGINEERING SCIENCE

AT

NEWARK COLLEGE OF ENGINEERING

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Newark, New Jersey

APPROVAL OF DISSERTATION

CONCEPTS IN LSI SERVO-CONTROL-ELECTRONICS

BY

ALFONS TUSZYNSKI

FOR

DEPARTMENT OF ELECTRICAL ENGINEERING

NEWARK COLLEGE OF ENGINEERING

BY

FACULTY COMMITTEE

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ABSTRACT

This thesis deals with the engineering aspects of control electronics. It examines modern concepts of servo-control theory in the light of recent developments in the technology of monolithic circuits. Applicational considerations are slanted towards Aerospace standards of reliability and power-consumption economy.

Conclusions drawn from the discussion of fabrication constraints and performance requirements lead to a preference for digital implementations. Yield probelms on one hand and aging effects on the other greatly reduce the feasibility rating of analog arrays.

Current practice in servo-control electronics revolves around purely analog implementations, sampled-data systems and primitive on-off arrangements. The motivation behind the status quo and the justification of the proposed approach are discussed in detail.

The organization of digital systems is examined in order to demonstrate the feasibility of Large Scale Integration (LSI) in servo-control electronics. The questions of hardware versatility and power-dissipation economy are emphasized from technological, economical and applicational standpoints.

Self-Contained loops and Computer-Aided systems are investigated within the ramifications of a functional division into Detectors, Compensators and Drivers. Differential Frequency Modulation is assumed to effect the information

transfer from the Pick-Off coil of the transducer to the Input ports of the Ratemeter. Pulse Width-Frequency Modulation is employed at the Driver-Torquer interface.

The operation of the Ratemeter conforms with classical logic, except for a slope-independent Level-Crossing-Discriminator (LCD), which is designed to provide a time-resolution gain of 3 db. over conventional frequency detectors. Circuit details of the LCD are given in order to illustrate differences between integrated and discrete circuit configurations. Two types of compensators are discussed: canonic pole-zero arrangements with ROM multipliers and Kalman filters with stored-program implementations of covariance equations.

The concept of Pulse-Width-Frequency-Modulation (PWFM) is introduced to reconcile the dynamic-range requirements of servo-control drivers with the time-resolution limitations of power transistors. Simple means of implementation of PWFM are also given; they take the form of a combination of logic-gates and DDA elements, a technique which could be used to advantage in other applications, especially digital detection and filtration.

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INTRODUCTION

Confrontation with a significant new device or phenomenon stimulates research in associated sciences and technologies. The ensuing effort is usually directed towards the development of the basic concept, the improvement of the fabrication techniques or the utilization of advantageous characteristics of the given device. Quite frequently disappointment follows because of technological problems, as witnessed in the case of multi-grid gas tubes, or applicatory difficulties, as in the case of tunnel diodes.

Occasionally the utility and feasibility of a discovery may become immediately established, evoking wide-front research into all pertinent aspects of technology and engineering. This has happened in the case of the Junction Transistor, the Integrated-Circuit (IC) and, most recently, in the case of the Large-Scale-Integration (LSI) technology.

The greatest concentration of IC and LSI oriented research is understandably found in areas associated with mass-production items such as digital-computer elements, operational amplifiers and functional modules for TV. Devices of lesser market potential do not receive much attention during the early stages of the evolution of the solid-state technology. There is, however, a noticeable trend towards an unprecedented level of standardization of individual devices and complete systems.

A stalemate situation prevails in the field of Servo-Control hardware. Current practice in Servo-Electronics is confined to analog implementations; there is a slow trend towards Central-Computer processing of all control data.

We intend to explore the implementation of Servo-Control-Electronics in the light of the possibilities presented by the LSI technology, without bias induced by common usage in other applications, but with recognition of the advantages of proper standardization.

We investigate, in Chapters I and II, the theoretical concepts, applicatory requirements and technological limitations of Servo-Electronics, and arrive at a preference for digital, rather than analog, implementations. Digital implementations are compatible with the fabrication constraints of LSI. They also meet the stability requirements of modern control installations. Analog implementations do not fulfill either of the above two requisites.

Organizational concepts and module-level details for the implementation of LSI Control-Electronics are presented in Chapters II through V.

CHAPTER I

SERVO-CONTROL ELECTRONICS--STATUS AND INNOVATIONS

Theory

The mathematical aspects of control-theory and associated subjects have received a good deal of attention during the last two decades. The "state-space" formulation of differential equations and the "state-transition-matrix" representation (H6, Z1, D3, S2, R8) of dynamic systems have attained the status of classical procedures. Optimization of filters progressed from the Wiener-Kolgomorov theory (L2, P3, W6) to the Kalman-Bucy realization (K3, K2, S12, F1), shifting the interest from the implementation of the Wiener-Hopf Equation to the solution of the Variance Equation. Popularization of topological methods diversified the approach to Active-Filter synthesis (B1, B2, P1), while the development of computerized analysis (H1, K8, D2) lightened the burden of network computations.

Bellman's Principle of Optimality (B4, B5, B6, T6) and Pontryagin's Minimum Principle (P7, T3, A4) led to new concepts of system optimization. Kalman's Theory of Duality (K1, K2, H3) linked stochastic filtration to deterministic optimal-control. The Z-transform became a standard tool of Sampled-Data analysis (F4, K7, L7) and Digital-Filter synthesis (K9, R1, B7). The Fast-Fourier-Transform algorithm (C7, B12, M3) revitalized spectral analysis and strengthened the already prevalent trend towards central-computer processing of all control-data.

Most of the above techniques can be grouped together under the heading of numerical methods in process control. The interest in these techniques has arisen in response to the popularization of digital computers, which have become everyday tools of human and machine operations. The proliferation of digital computers is in turn attributable to recent developments in solid-state physics.

There are applications in which general-purpose computers do not present the best engineering solution. Time-sharing is not a panacea, not even in large installations. Some specialized problems can be solved by relatively modest means. Analog methods are acceptable in many short-duration projects.

It is therefore necessary to investigate which functions can be best performed by analog and which by digital hardware. In the digital domain one must further discriminate between special-purpose hardware and central-computer implementations. We will deal with the above problems within the ramifications of Servo-Control-Electronics.

Technology

The first semi-conductor amplifying device, the point-contact-triode (B3), did not progress beyond the level of a demonstration model, but Shockley's invention of the junction-transistor (S9, S11) has produced practical results. It has also established a principle of lasting value and utility.

The junction-transistor was initially fabricated as a grown-junction device. In an attempt to boost the frequency response and to streamline fabrication techniques, other structures and processes (V1, K6, G3) were tried with various degrees of success. A major innovation by Hoerni led to the planar transistor (H4) and the passivation techniques (P6), which are in general use today. The epitaxial process (C3, B13, M6), a breakthrough in crystal-growth technology, widened the performance horizons of discrete transistors and provided a workable basis for the fabrication of integrated-circuits. A good deal of present-day research is devoted to ion-implantation techniques (L3), which are expected to improve the controlability of the doping process.

Integrated-Circuits are a natural outcome of the planar technology. Contemporary IC's are generally made by the six-masks process (W1). Some new ideas have been introduced to overcome the drawbacks of the bi-polar IC technology: buried-layer diffusion (G2) to reduce the collector-resistance, and lateral-transistors (M8) as well as substrate-collector transistors (S3) to replace conventional pnp devices. Diode isolation continues to maintain a dominant position by virtue of its simplicity and efficacy.

The development of practical field effect devices has been retarded by various surface state problems (M11, W4). Threshold instability and general lack of dependability are still the worst drawbacks of MOS transistors, but steady progress in oxide formation and etching techniques (M7, M1) begins to yield devices which are compatible with LSI concepts and requirements. MOS devices can be

integrated without isolation. One simple structure can be used either as a transistor or a resistor. Slight modification of the pattern gives a capacitor. Multi-Phase logic (K4, Y1) overcomes the speed limitation of RC circuits. Complementary MOS arrangements (R4, L9) produce even better results, admittedly at the expense of technological complications.

Our concept of LSI is predicated on the use of multi-layer interconnect matrices (L10). The first layer interconnects separate devices into logic-elements such as gates, flip-flops, shift-registers, etc. The second layer assembles the logic-elements into modular groups such as counters, adders and multipliers. The third metallization layer, if used, converts modular groups into sub-system blocks at the level of scratch-pad memories, arithmetic-units, canonic filters and ratemeters (L5).

A three-sided comparison between bipolar, complementary MOS and multi-phase MOS implementations would appear to be in order, but an examination of the third technique with regard to long-term objectives reveals the distinct stigma of a stop-gap measure. It is, therefore, advisable to confine our comparison to the bipolar and the complementary MOS technologies.

Bipolar devices have a clean-cut advantage in speed (H2, L10); LSI blocks of Emitter-Coupled-Logic operate at nano-second clock-rates (W7). Furthermore, junction transistors are still more stable and more reliable than MOS-FETs. Their intrinsically high transconductance (W2) is useful in sense-amplifier applications.

MOS arrays have excellent speed/power characteristics (A2), facilitating operation of mega-Hertz gates at nano-Watt power levels. They are also very economical in terms of substrate-area (F2).

The choice between the two techniques depends on applicatory factors. In Servo-Control-Electronics speed requirements are modest, but reliability considerations dictate the choice of bipolar techniques. As the stability of MOS devices improves, FET implementations may become preferable because of power-economy considerations.

The LSI technology has its due share of disadvantages. There are power dissipation difficulties, interconnection problems, standardization requirements, tolerance limitations and some economic complications.

The first two disadvantages of LSI are inherent in the miniaturization concept. As we shrink the dimensions of a device, we reduce its power dissipation rating and impose limitations on the size and number of terminals.

Other disadvantages are attributable to the empirical status of the semi-conductor technology. The end result of a series of operations embracing crystal formation and surface preparation as well as a number of etching and diffusion operations cannot be expressed by a mathematical formula. We must therefore rely on conformance with empirically established procedures. Repeatability of device characteristics is the sole criterion of process control.

The reliability of monolithic circuits can be very high (W3, M9) if mass production methods are combined with (1) stringent in-process inspection, (2) far-reaching electrical characterization, and (3) extensive follow-up testing. On the other hand, reliability will be poor, or at best indeterminate, if small-batch lots are produced under conventional laboratory conditions.

Reliability of low-demand items presents a problem which is especially severe in servo-control-electronics. The demand for any particular type of servo-control-hardware is quite low in terms of IC-production quantities. It is therefore necessary to devise a scheme which will embrace a large section of the total servo-control market, and thus create a demand compatible with IC-fabrication economics.

Product standardization plays an important role in LSI science and economics. It boosts the yield and cuts the costs while it improves reliability and electrical performance, but it demands specialization and resourcefulness. Individual circuits must be sufficiently versatile to work in conjunction with a wide variety of other circuits and the performance of generic families must be sufficiently good to meet the requirements of many applications.

Circuit Design

The last 15 years have witnessed two major evolutions of circuit-design concepts. The first marked the transition from electron-tube to transistor circuits; it reached its peak at the turn of the decade, when it became apparent that the advent of the Silicon-Planar

technology (H4) had produced the best available amplifying device. Many new circuit-configurations emerged, some utilizing unique advantages, others overcoming unique limitations of the transistor-technology. There was a significant increase in the number of active devices per circuit and a decrease in the number of passive devices. On the system level, a slight preference for digital implementations became noticeable.

Popularity of thin-film resistor-matrices in the early sixties (T9) brought only minor changes in the approach to circuit design. However, since it coincided with an intensification of research work in Active Filters, it helped to eliminate the use of magnetic components in compensator applications.

The second evolution, much more drastic than the first, was set off by the emergence of the monolithic-circuit technology. Preference for digital implementations moved up another notch and circuit design began to merge with device design.

In analog circuits, some of the new arrangements arose from an observation disclosed by us in 1962 (T8) and extended by Hoffait and Thornton in 1964 (H5). This observation concerns the thermal drift of dual-transistors and states that the thermal coefficient of the offset-voltage is proportional to the offset-voltage itself.

Let ΔV be the offset-voltage of two generically similar transistors, then

$$d(\Delta V)/dT = d(V_{be1}-V_{be2})/dT = k(\Delta V) \qquad (1)$$

where,

$k \approx 3$(microVolts/°C) per milliVolt of offset, if (2)

$I_{c1} = I_{c2}$ and $V_{ce1} = V_{ce2}$.

Practical utilization of this principle in Integrated Circuits is predicated on the intrinsic matching of devices contained within one die. Matching to better than 1/2mV-offset is typical, permitting implementation of simple constant-beta structures (W9, W11) and transistor-controlled current-sources (B10).

In digital circuits, development of multiple-emitter transistors produced the popular TTL gate (L10). Utilization of the predictability of charge-storage ratios brought about the MTTL III family (M10). However, most conspicuous is the abundance of active elements, even in modest-performance circuits. Whereas a discrete component flip-flop may contain 4 to 8 active elements, an integrated flip-flop contains at least 30 transistors. The Level-Crossing-Detector, shown in figure III.2 as an example of IC design, comprises 11 transistors and 8 resistors, or 1.37 transistors per resistor.

Transition to Large-Scale-Integration does not provide any benefits at the circuit level. On the contrary, it imposes a number of design and fabrication constraints. Nevertheless, further circuit-research is required in order to utilize the sub-system advantages of LSI. The speed of digital modules is no longer limited by the parasitic effects of interconnection wires. It is therefore desirable to develop picosecond logic.

Applications

Microscopic size may be the most spectacular feature of monolithic circuits, but there are other equally important characteristics. Their utility depends on applicatory requirements. To deal with LSI implementations of Servo-Control-Electronics, we have selected Aerospace applications. These applications call for a combination of features such as small size and low power consumption as well as high reliability and long-term stability, and thus display the entire spectrum of the advantages and limitations of molecular electronics (T7, J1, L5).

Current practice in servo-control-electronics is essentially restricted to analog implementations. A typical system may contain 8 integrated amplifiers, 10 discrete transistors, 6 micro-Farads of capacitors and a few discrete resistors. The quality of a set of hardware is determined by its frequency response, gain stability, offset-voltage and offset stability, general reliability, power consumption, mechanical factors and modular organization.

In typical designs, frequency response and gain-stability requirements do not present any difficulties, but offset-voltage and drift specifications do create some serious problems. We have learned to deal with thermal drift (W9, H5, T8), but we are still unable to cope with the offset-voltage and aging problems, except by MOS-chopper stabilization, a bulky and conceptually clumsy technique. Initial errors and aging effects are beyond the control of circuit designers. These are technological problems, the former being

determined by the quality of the passivation techniques (M1, M7) and the latter by the tolerances of the masking and etching processes. The best available operational amplifiers display offsets of the order of 2 milli-Volts; aging drift of the offset voltage may exceed 5 milli-Volts per year.

Periodic adjustments constitute the only practical but highly objectionable solution of the offset-voltage problem. First, because a military system may be called to instant action after years of storage, and there may not be any time nor opportunity for extensive calibration procedures. Second, because the incorporation of adjustment accessories degrades the reliability of the system, opening a Pandora's box of failure possibilities.

Many malfunctions and catastrophic failures of electronic circuits can be attributed to accidental overloads inflicted during the performance of calibration adjustments (V3). If damage does occur, a chain reaction may follow. Undetected partial damage may induce a catastrophic failure at a later time. Detected damage may bring forth all sorts of complications invariably associated with retrofit operations.

Reliability being the most pressing issue in Aerospace electronics, it is clearly necessary to reduce offset errors to acceptable levels. Initial-offsets could be eliminated, at least in theory, by a yield trade-off, but nothing significant can be done about the long-term drift of analog circuits. At fault is the basic principle of analog circuits, the "principle of voltage proportionality."

To eliminate aging effects we must turn to the "threshold principle" of digital circuits. We can then proceed to realize the full reliability potential of LSI arrays by elimination of all unessential terminals and by provision of short-circuit protection on all interface gates. Where reliability requirements are exceptionally stringent, we can exercise the option of redundance techniques, easily implementable in digital circuits (majority voting) but unfeasible in analog circuits.

CHAPTER II

ORGANIZATION OF THE ELECTRONIC SUBSYSTEM

Analog Systems

Simplicity is the dominant feature of conventional analog control systems. The electronic subsystem of a typical control-loop (Figure II.1) comprises a Detector, a Compensator and a Driver.

The detector, functionally a phase-sensitive rectifier, usually contains a push-pull amplifier, two chopper transistors, two coupling capacitors and a few discrete resistors.

The compensator may resemble the arrangement of Figure 6 of Appendix III. Its configuration depends both on the order and the values of the coefficients of the transfer function.

The driver is, as a rule, a class B amplifier; discrete power-transistors are generally used in the output section, although an experimental version of a monolithic driver had been fabricated in 1966 (R7).

Refinements may be introduced in one or more modules to comply with requirements of special applications. Where relatively sophisticated control is to be implemented or information interchange between various elements of a major installation is required, recourse can be taken to Sampled-Data techniques.

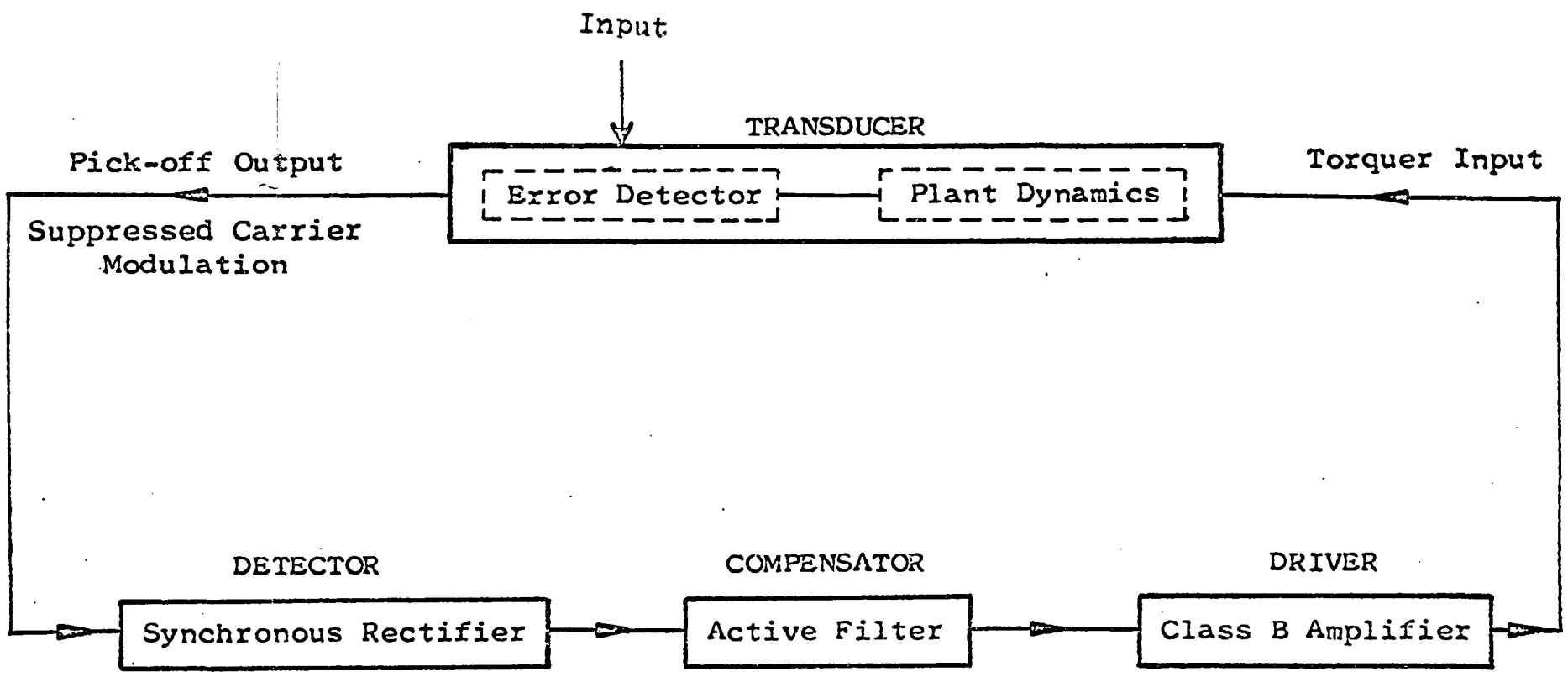


FIG. II.1: AUTONOMOUS ANALOG SYSTEM.

The block-diagram of a Sampled-Data-System is shown in Figure II.2. It is evident that an Analog-to-Digital converter is necessary to translate analog data into the language of the digital computer, but it is not intuitively obvious that a low-pass filter must precede the converter.

The frequency spectrum of a uniformly sampled signal (R2, P4, J2, F4) is:

$$F^*(jw) = \sum_{r=-\infty}^{\infty} F(jw + j2\pi r/T) \tag{1}$$

where:

$F(jw)$ = Fourier transform of the original signal,

$1/T$ = Sampling rate,

r = Dummy integer.

Thus, there is a simple relationship between the frequency spectrum of a sampled signal, $F^*(jw)$, and the frequency spectrum of the original, continuous signal, $F(jw)$, if the spectrum of $F(jw)$ is contained within the limits:

$$|w| < \pi/T, \tag{2}$$

in other words if

$$F(jw) = 0 \text{ for all } |w| > \pi/T \quad \text{(see Figure II.3).} \tag{3}$$

If, however,

$$F(jw) \neq 0 \text{ at any } |w| > \pi/T \tag{4}$$

then $F^*(jw)$ becomes distorted by overlap of excess frequencies. This phenomenon, called "aliasing" (C4), necessitates the use of a low-pass filter.

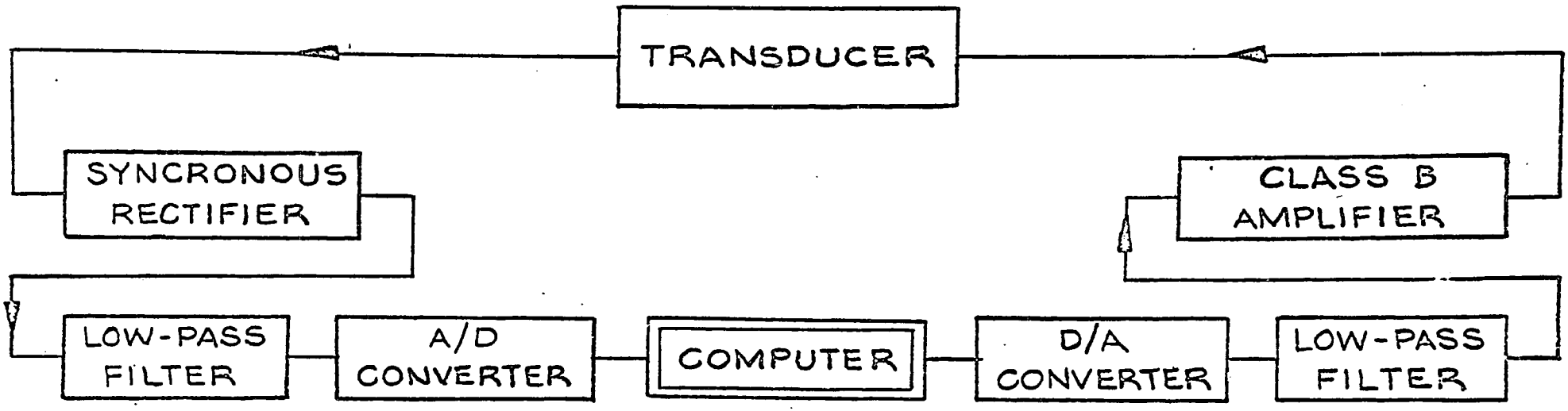


FIG.II.2: SAMPLED DATA SYSTEM.

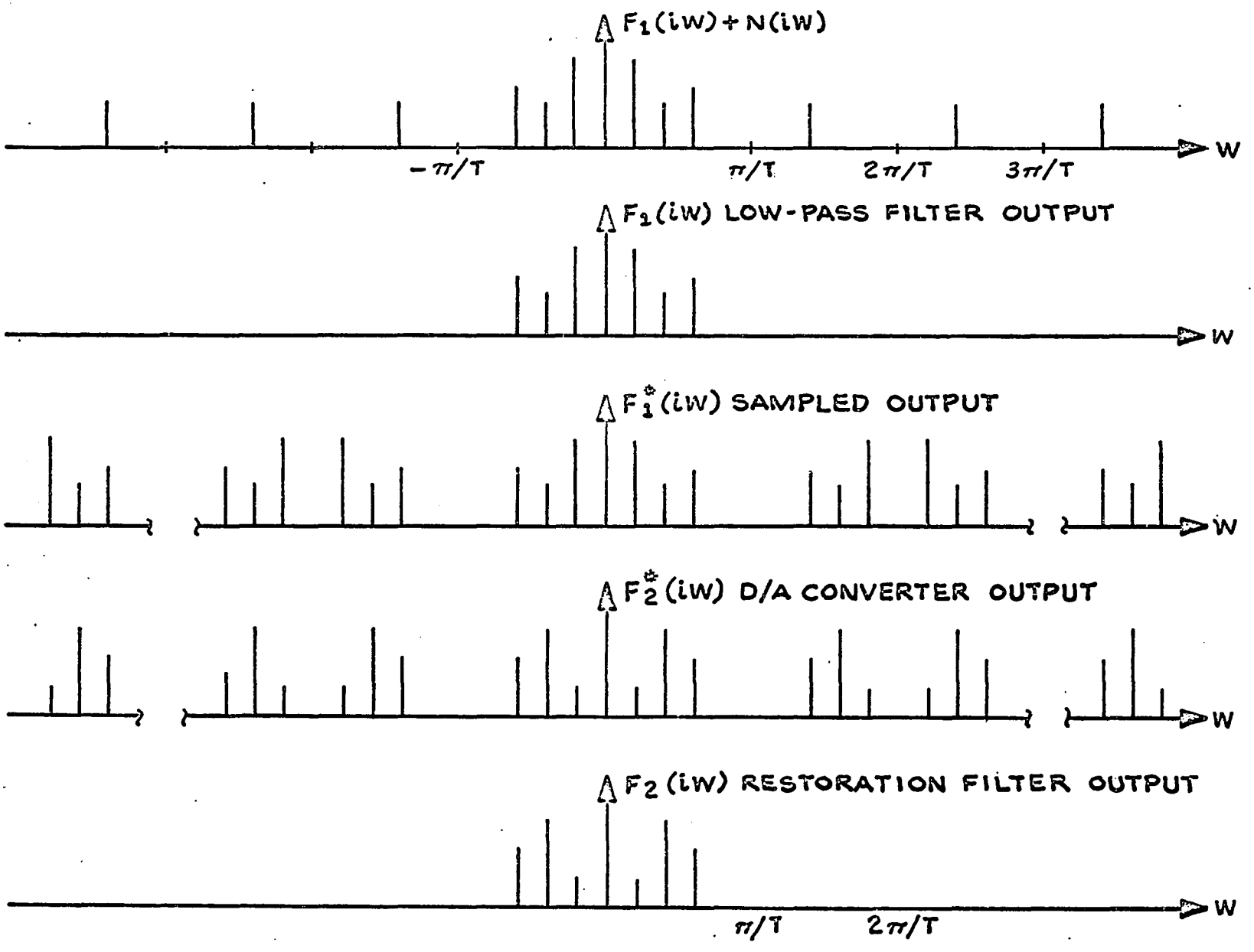


FIG. II.3: THE SAMPLING-PROCESS SEQUENCE

Theoretically speaking, the low-pass filter would not be necessary if the input signal was known to be contained within the fundamental band defined by equations (2) and (3). However, in engineering deliberations one must recognize the existence of noise, and look upon equation (1) as a demonstration of noise-susceptibility. Although low-frequency noise is expanded in the same fashion as the signal, aliasing of high-frequency noise increases the noise-energy-content of the fundamental band. It is, therefore, necessary to use the low-pass filter in all practical applications.

The Central Computer of the system, performing the function of a presumably complex compensator, transforms $F^*(jw)$ into another function $G^*(jw)$, in accordance with some predetermined equations.

To examine the restoration process, we observe that elimination from $G^*(jw)$ of all frequencies outside the fundamental band enables us to equate the Fourier-Integral representation ($G(jw)$) with the corresponding Fourier-Series representation and thus to arrive at the identity:

$$g(t) = \sum_{k=-\infty}^{\infty} g(kT) \frac{\sin.\ \pi(t - kT)/T}{\pi(t - kT)/T} \tag{5}$$

where:

$$G(jw) = 0 \text{ for all } |w| > \pi/T \tag{6}$$

$G(jw)$, $g(t)$ are Fourier integral pairs

k = Dummy integer

Equation (5), known as the Sampling-Theorem (S1, S7, L1), explains the need for the restoration filter at the output end of the D/A converter. It contains the essence of all SDS operations, and states that a function g(t) is uniquely represented by its values at uniformly spaced instants, provided that G(jw) complies with equation (6).

The events which take place during the execution of a sampling cycle are portrayed in Figure II.4. A somewhat artificial example has been chosen for the sake of clarity.

Summarizing this section we recall the simplicity and component-economy of self-contained analog control-loops. We also note that extension of analog concepts to Sampled-Data-Control introduces a number of complications, resulting from the basic incompatibility of digital and analog techniques.

Digital Systems

Figure II.4 shows the block diagram of a self-contained digital loop. As in the corresponding analog system, there are three functional modules, a Detector, a Compensator and a Driver. The operation of the three modules is coordinated by a system clock which is usually contained within the central-computer complex.

The circuit arrangement of the electronic detector depends on the principle of operation of the transducer. In some cases the detector can be omitted entirely, in others it may be sufficient to provide a code converter. The error detector of the transducer

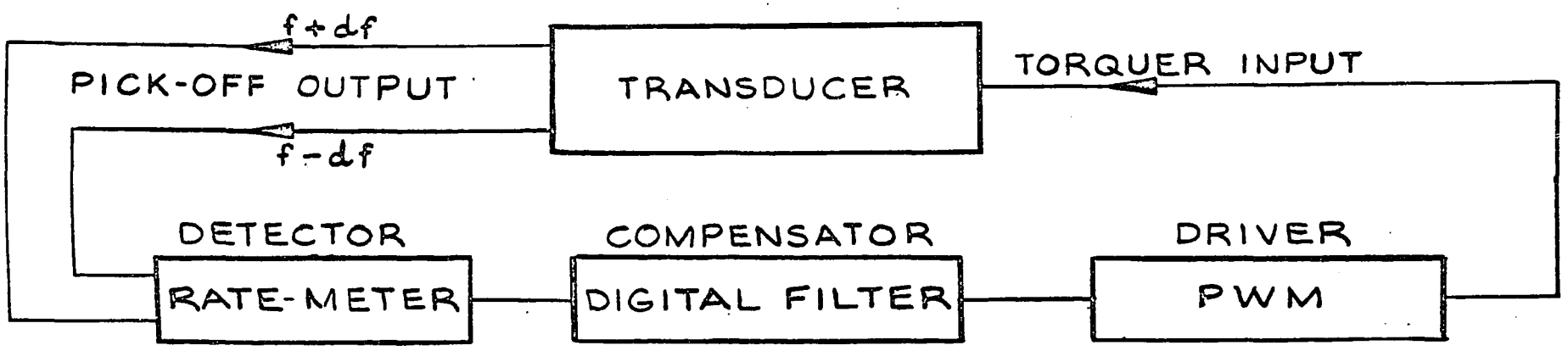


FIG.II.4: AUTONOMOUS DIGITAL SYSTEM.

considered in this thesis is assumed to respond in the differential-frequency-modulation mode, generating two signals, one characterized by the frequency $f_o + df$ and the other by $f_o - df$. The electronic detector takes, therefore, the form of a differential ratemeter. Its output is proportional, or nearly proportional, to the deviation ratio df/f_o.

The configuration of the remaining two modules is independent of the error detection mechanism. The compensator may contain canonical pole-zero elements (D1), or a Kalman filter, or both. The topological complexity of the driver depends on linearity specifications but the proposed PWFM driver will meet all rational requirements.

Structural details of the three modules are discussed in Chapters III to V. Implementation of any one of these modules requires far more components than the implementation of an entire analog system, but the quality of the digital components need not be as high as the quality of the analog components.

The block-diagrams of two computer-aided control systems are given in Figure II.5. In Figure II.5a, all compensation functions are performed by the central computer. In Figure II.5b, the central computer controls the operation of the local compensator by periodic adjustment of its coefficients (Chapter IV).

The simplicity of the computer-aided arrangements stands in striking contrast to the complexity of Sampled Data Systems, which

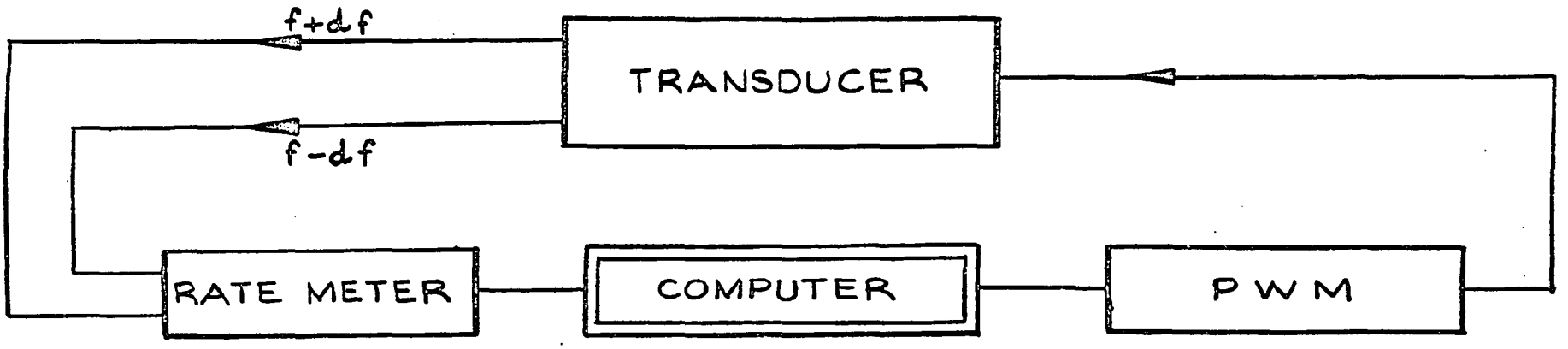


FIG.II.5a: COMPUTER AIDED DIGITAL CONTROL.

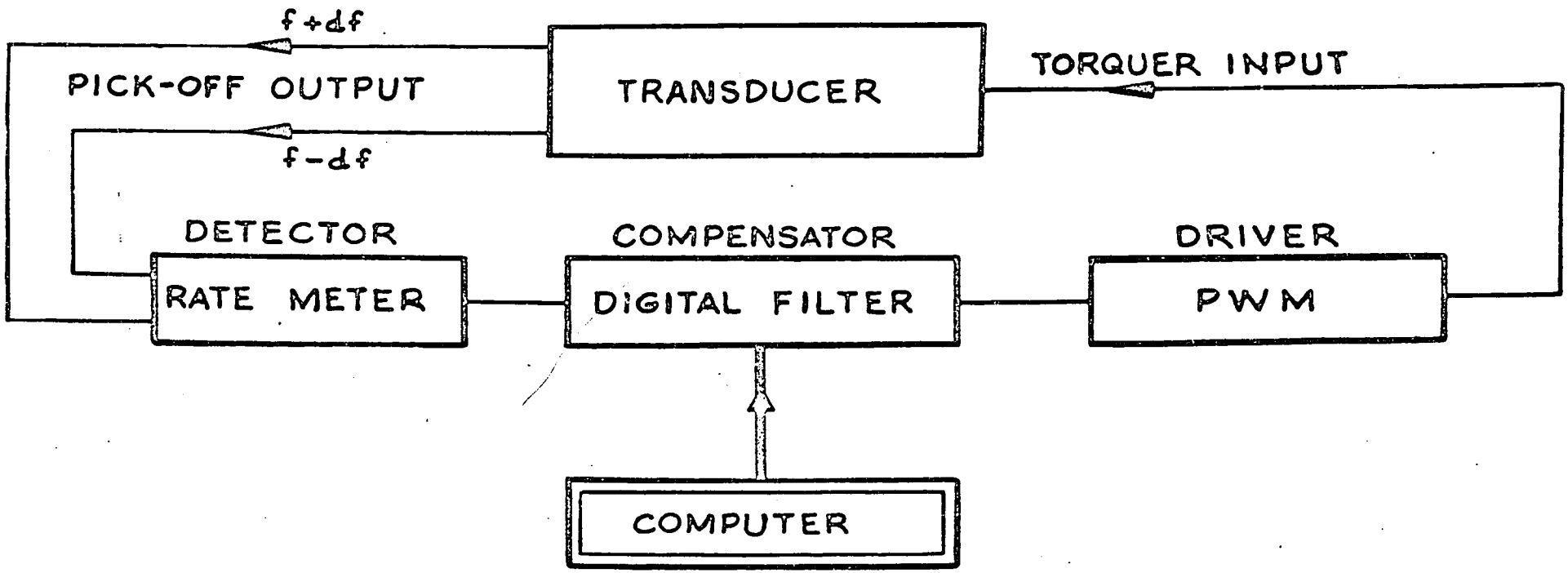


FIG.II.5b: ADAPTIVE LOOP.

carry the burden of conceptually redundant hardware. All digital modules can be completely compatible. There need not be any difference between Ratemeters for autonomous loops and Ratemeters for computer-aided loops. The same applies to Drivers and other auxiliary equipment.

The Digital vs. Analog Decision

The main arguments in favor of digital techniques in servo-control-electronics can be listed as follows:

1. Compatibility with the general trend in control theory.
2. Reliability and immunity to moderate aging effects.
3. Compatibility with the state of the art in Silicon Technology.
4. Simplicity of Adaptive-Control implementations.

There are two significant arguments for analog techniques, namely tradition and component economy.

Although some of the disadvantages of analog implementations are sufficiently severe to disqualify analog concepts from all LSI considerations, it would be unwise to overlook the possibility of compromise solutions. We cannot ignore the question of current practice in servo-control electronics. To present a complete argument in favor of digital techniques, we must explain why analog techniques are being used at present.

Component economy is the main reason behind the past and present popularity of analog implementations. The analog double-pole,

double-zero active filter of Figure 6 of Appendix III consists of one amplifier, two capacitors and five resistors. An equivalent 11-bit digital filter would require twenty-two Delay Flip-Flops, two 11-bit, 4-input adders and five 11-bit multipliers; evidently, realization of such filters in terms of discrete transistors is unfeasible, except for demonstration purposes. The choice between digital and analog hardware was only brought about by the emergence of integrated circuits.

The criterion of component economy, which dominated the approach to circuit design until recently, has been deflated by LSI; more important are the questions of component quality, margins against malfunctions and susceptibility to parasitic oscillations (C1, P5).

Where reliability, long-term stability or sophistication are important, digital LSI presents the only rational solution. Analog techniques will be used in various hybrid implementations of non-critical systems for a few years to come, but they will be eventually eliminated by economic factors, even from these applications.

The remainder of this thesis will be devoted to the realization of ratemeters, digital-filters and pulsed drivers, with particular attention to applicatory diversity and modular compatibility.

CHAPTER III

DIGITAL DETECTORS

Principle of Operation

The digital detector generates a binary output in response to two sinusoidal or square-wave inputs. The output of the detector represents the frequency-deviation-ratio of the input signals.

The principle of operation of the proposed detector is portrayed in Figure III.1.

Two input signals, characterized by frequencies $f_o + df$ and $f_o - df$, are respectively fed into two Level-Crossing Discriminators (LCD-A and LCD-B). The discriminators generate two pulse trains, one at a repetition rate of $2(f_o + df)$ and the other at $2(f_o - df)$.

While the Inhibit-Gates (F3, H7) are open, the pulses flow into two counters (P8, G1) until saturation occurs in the counter with the faster input. The saturation event shuts the Inhibit-Gates; it also feeds the complement of the other counter into the Output-Register.

Assuming relaxation of both counters at $t = 0$, the overflow event will occur at time

$$t_x = \frac{N}{2(f_o + df)} = \frac{N}{2f_o(1 + x)} \tag{1}$$

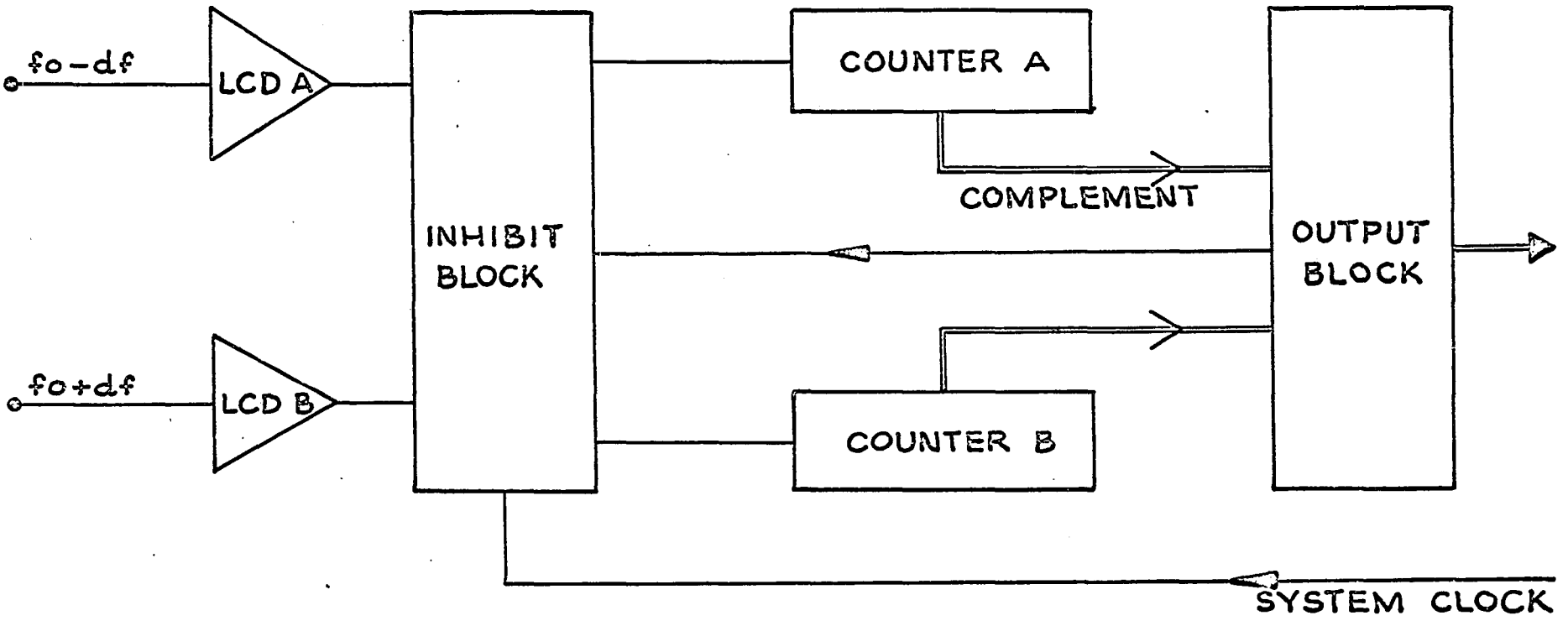


FIG. III.1: DIGITAL DETECTION OF DIFFERENTIAL FREQUENCY MODULATION

where:

$N = 2^n - 1$ = Capacity of each of the counters. (2)

n = Number of storage elements in each counter.

$x = df/f_o$ = Frequency-deviation ratio. (3)

The state of the other counter at time t_x is

$$m = 2t_x(f_o - df) = 2t_x f_o(1 - x)$$

$$= N\frac{1 - x}{1 + x} \tag{4}$$

The complement of m is equal to $\bar{m}$,

$$\bar{m} = N - m \tag{5}$$

$$= 2xN/(1 + x) \tag{6}$$

or,

$$x = \frac{\bar{m}}{2N(1 - \bar{m}/2N)} \tag{7}$$

Equations (6) and (7) give the relationship between x, the frequency-deviation-ratio, and $\bar{m}$, the output read-out of the detector. At low deviation ratios, the read-out is proportional to x,

$$\bar{m} = kx \qquad (x << 1) \tag{8}$$

Noteworthy is the fact that f_o appears in equation (6) only in the form of the deviation ratio df/f_o. This means that the read-out of the ratemeter is independent of f_o, if the sensitivity of the transducer is independent of f_o.

The Level-Crossing-Discriminator

The schematic diagram of a new type of Level-Crossing-Discriminator is presented in Figure III.2.

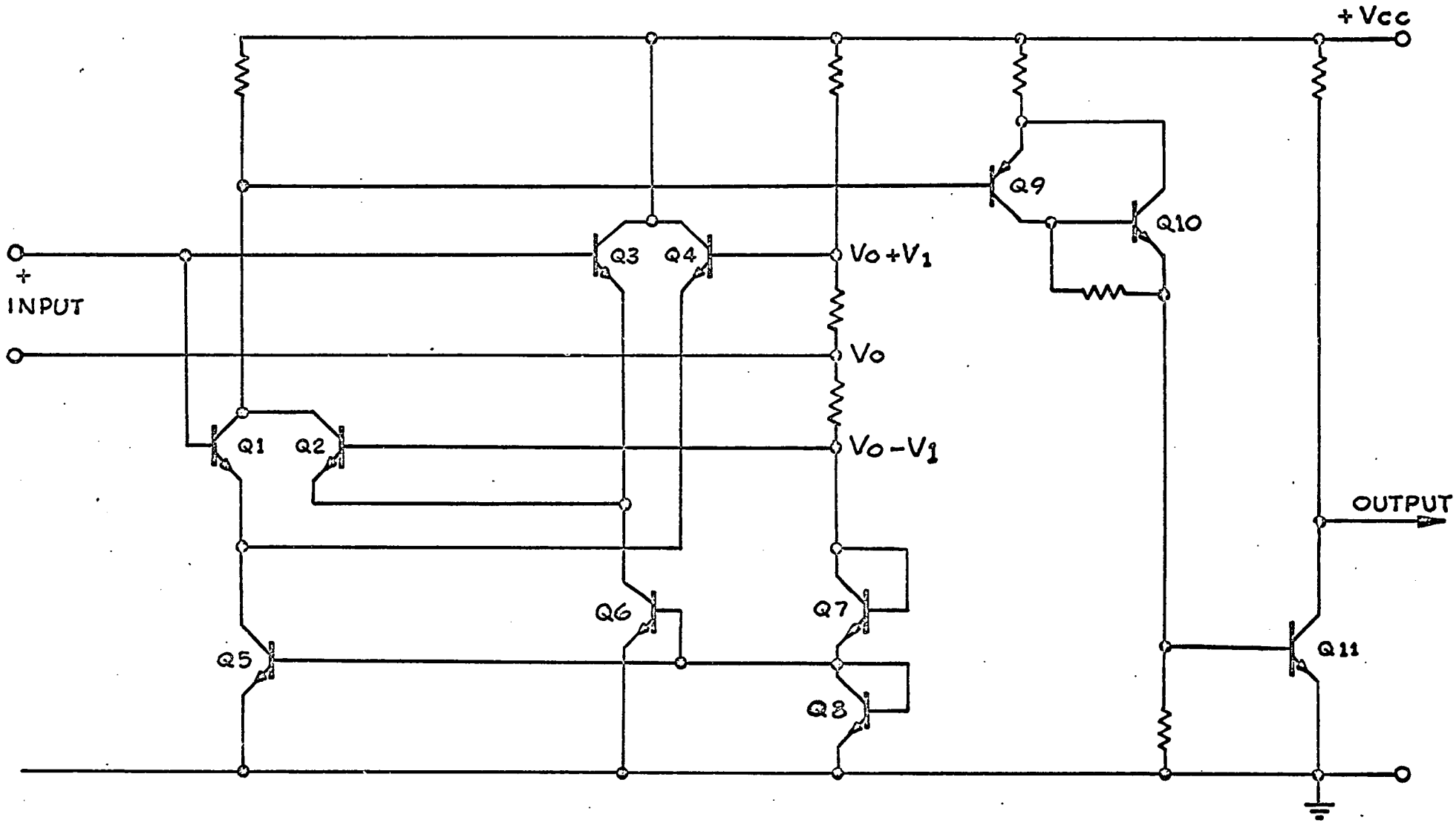


FIG.III.2: LEVEL CROSSING DISCRIMINATOR

Transistor Q_1 conducts whenever the input voltage exceeds V_1, transistor Q_2 conducts when the input voltage drops below $-V_1$. Thus, the voltage at the common collector of Q_1 and Q_2 is low, except when the input voltage falls within the limits:

$$-V_1 < V_{in} < +V_1 \tag{9}$$

The output voltage (V_o) conforms, therefore, with the following equations:

$$V_o = \text{Low}, \quad \text{when} \quad V_{in} > |V_1| \tag{10}$$

$$V_o = \text{High}, \text{ when } -V_1 < V_{in} < +V_1 \tag{11}$$

Under normal operating conditions, the amplitude of the input signal is considerably larger than V_1. Consequently, a positive output pulse is produced whenever the input signal crosses zero in either direction. The output pulses are centered on $V_{in} = 0$. Their width depends on the amplitude and shape of the input signal.

Compared to conventional Sense-Amplifiers (T1, T2, W10), the proposed LCD has two advantages. It has a better time-resolution, since it generates output pulses both at the positive-going and at the negative-going crossings of the zero-voltage level. Also, it produces pulses of optional width instead of the square-waves associated with Sense-Amplifiers.

The schematic diagram of the LCD discloses a few features which are peculiar to Integrated-Circuit designs. It has 8 resistors and 11 transistors, or less than one resistor per transistor. The common-collector devices Q_1Q_2 and Q_3Q_4 combine surface-area economy

with metallization-pattern simplicity. The current sources Q_5 and Q_6 are controlled by the emitter-collector voltage of a transistor (Q_8) whose base is shorted to the collector. The compound emitter-follower (Q_9 - Q_{10}) overcomes the beta limitations of lateral pnp transistors.

The above LCD is intended only for operation with sine-wave inputs. In applications utilizing square-wave inputs, the LCD would be omitted or replaced by some pulse-shaping network, if necessary.

The Ratemeter

The block diagram of the ratemeter section of the detector is given in Figure III.3. It shows a half-adder (P9), some control logic and two counters.

The operational cycle of the ratemeter can be broken down into three action periods:

0,1 The externally controlled "synchronization pulse" resets the counters and enables input gates G1 and G2.

0,2 Incoming pulses are fed into the counters.

0,3 At $t = t_x$, one of the counters saturates (minterm = $2^n - 1$), inhibiting the input gates.

1,1 At $t = T$, the "synchronization pulse" initiates the next operational cycle.

During the time interval from t_x to T, gate K1 is in the "true" state, thus indicating the availability of output data. The Boolean equation of K1 is:

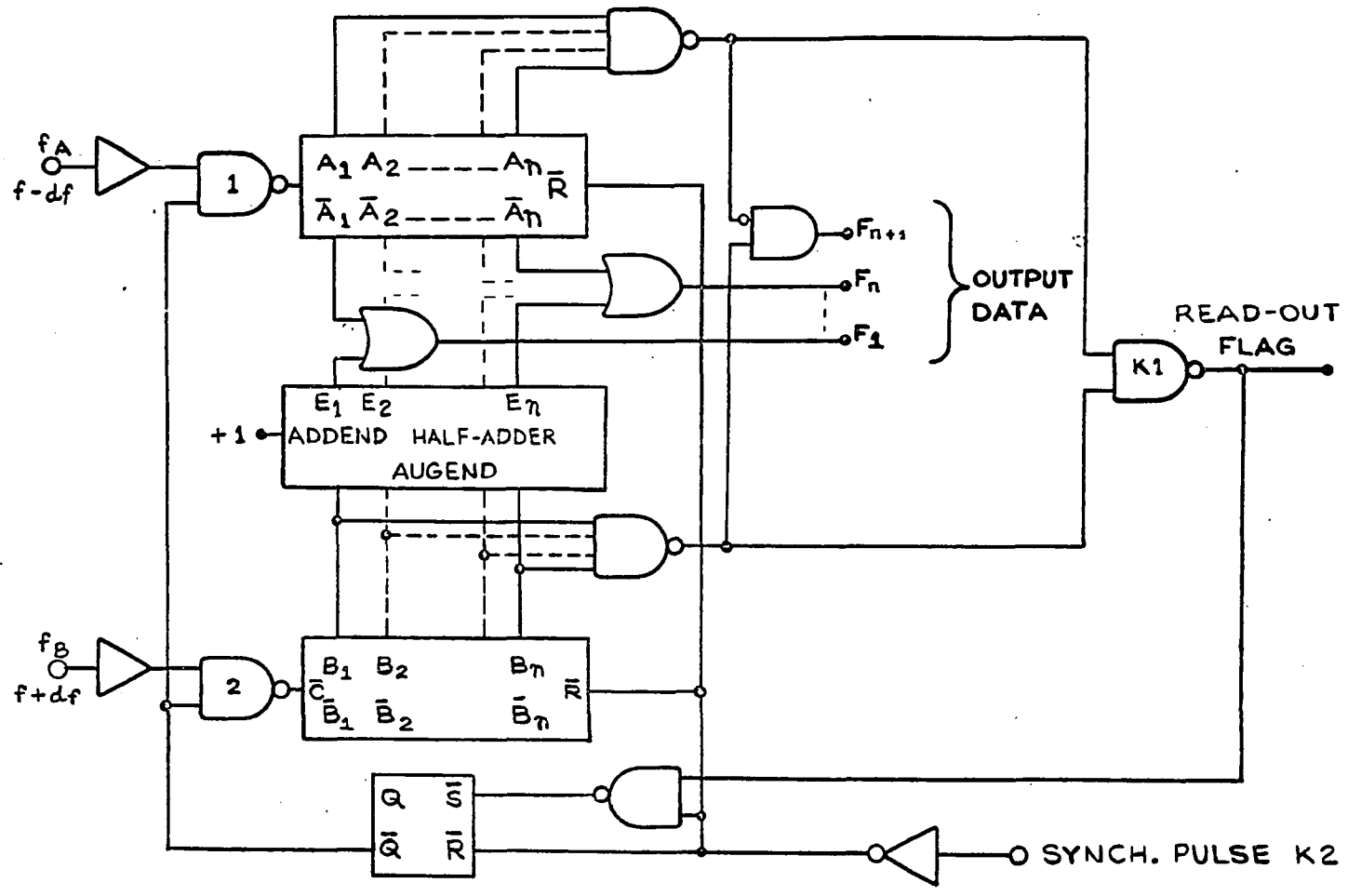


FIG.III.3: THE RATEMETER

$$K1 = \prod_{i=1}^{n} A_i + \prod_{i=1}^{n} B_i \tag{12}$$

The inhibit flip-flop is controlled by K1 and the external synchronization pulse K2, in accordance with the equations

$$S = K1\bar{K}2 \tag{13}$$

$$R = K2 \tag{14}$$

The half-adder is used for two's-complement coding of negative deviation ratios. To unravel the coding mechanism, assume that df, as shown in Figure IIL3, is negative.

In a normal operating cycle counter A will saturate first, forcing gate F_{n+1} into the true state and thus indicating that the deviation ratio is negative.

Gates F_1 to F_n are then supposed to display the negative equivalent of the complement of the state of counter B. In other words, we want the <u>two's-complement</u> of

$$\bar{B}_n\ \bar{B}_{n-1}\ \bar{B}_{n-2} \quad \ldots.\bar{B}_2\ \bar{B}_1.$$

The <u>one's-complement</u> of the above number is obviously given by

$$B_n\ B_{n-1}\ B_{n-2} \quad \ldots.B_2\ B_1.$$

To get the two's complement code, we add unity to the minterm of B, and thus obtain:

$$\text{minterm}(E) = \text{minterm}\ (B) + 1 \tag{15}$$

The problem of selecting the output information from either channel A or channel B does not exist, since all $\bar{A}_i$s are zero when any of the E_is are different from zero, and vice versa. We can thus

combine them by simple "or" gates, operating in accordance with the Boolean equation (T5, S4, C8, F3)

$$F_i = \bar{A}_i + E_i \tag{16}$$

Although f_o does not enter into equation (6), it is necessary to impose certain restrictions on the values of f_o and T, in order to ensure proper operation of the ratemeter. Obviously, t_x, the time to load the counter, must be shorter than T, the period of the synchronization pulses. Hence,

$$T > 2^n/f_o \tag{17}$$

for ratemeters working in conjunction with conventional sense amplifiers and

$$T > (2^{n-1})/f_o \tag{18}$$

for ratemeters working in conjunction with the LCD.

The proportionality-error in equation (8) must be considered in relation to the quantization-error, which is equal to the least-significant-bit of the output word. The transient behavior of the ratemeter resembles the behavior of a low-pass filter with a cut-off frequency of 1/T.

The above proposed detector can be used as a mixer-detector of conventional FM data, if a Local Oscillator is added to the arrangement of Figure III.1. The frequency deviation ratio of single channel FM signals is equal to

$$x = \frac{\bar{m}}{N(1 - \bar{m}/N)} \tag{19}$$

CHAPTER IV

DIGITAL COMPENSATORS

Digital processing resembles the sampling operation. Both techniques are discrete-time procedures which handle data collected at specific instants of time. The clock period of digital systems corresponds to the sampling period of sampled-data systems.

It is, therefore, convenient to apply to digital systems the difference-equation and Z-transform methods, which are generally used in sampled-data systems.

The Canonical Filter

A difference equation of the type

$$(1 + b_1E^{-1} + b_2E^{-2} \ldots + b_nE^{-n})y = (a_o + a_1E^{-1} \ldots + a_mE^{-m})x$$

where:

E^{-1} = Delay Operator (1)

can be implemented as shown in Figure IV.1. It can also be written as

$$y = \frac{A}{B} x \tag{2}$$

and expanded by introduction of an intermediate variable w, such that

$$w = \frac{x}{B} \tag{3a}$$

$$y = Aw \tag{3b}$$

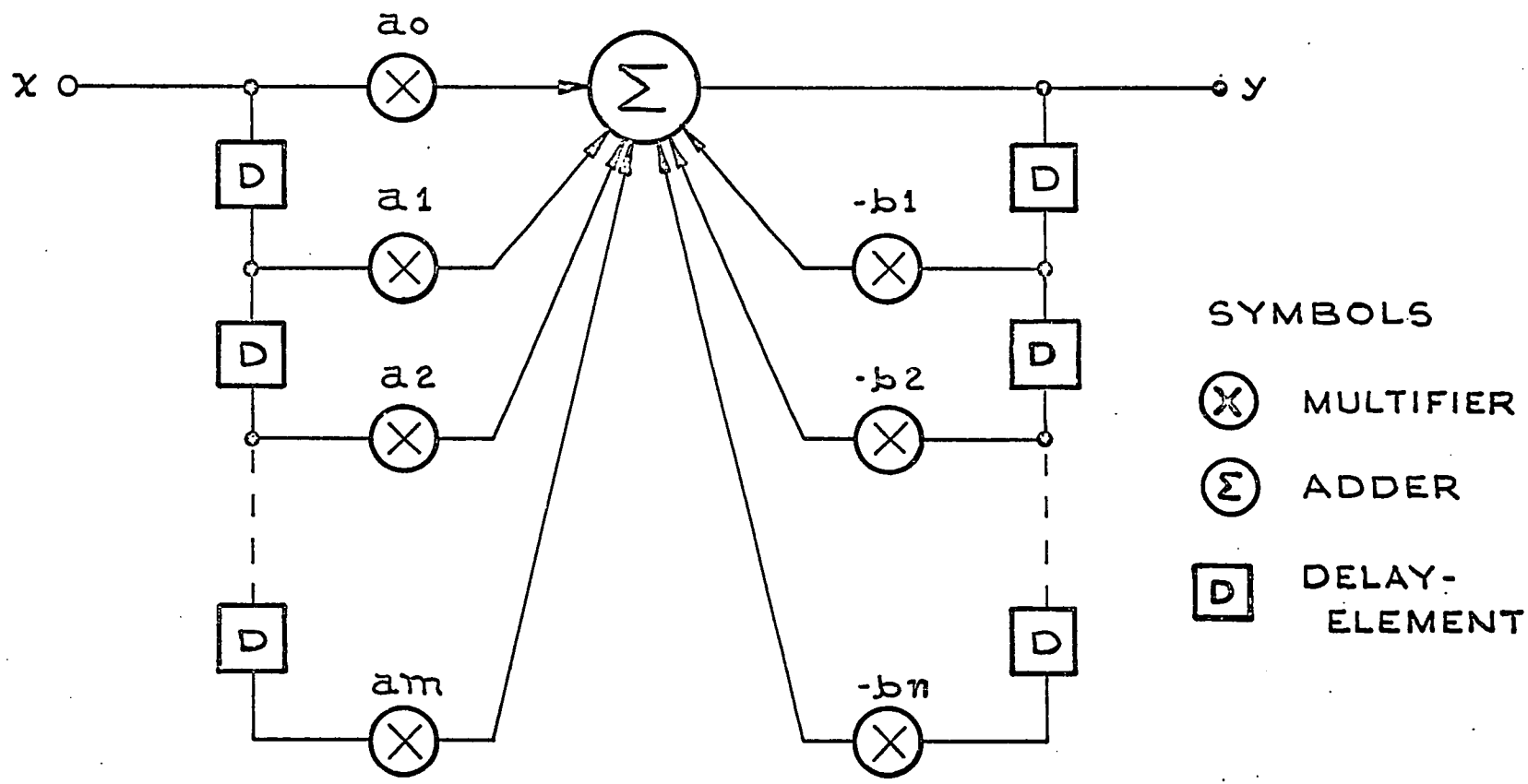


FIG. IV.1: IMPLEMENTATION OF EQUATION V.1

Development of equations (3) and (4) gives

$$w = x - (b_1E^{-1} + b_2E^{-2} + \ldots\ldots b_nE^{-n})w \tag{4}$$

$$y = (a_o + a_1E^{-1} + a_2E^{-2} \ldots\ldots + a_mE^{-m})w \tag{5}$$

Equations (4) and (5) suggest the implementation of Figure IV.2, sometimes called the "canonical filter" (D1, C5) because it employs the minimal number of delay elements.

Examining Figures IV.1 and IV.2, we discern three basic components of digital filters namely delay-elements, multipliers and adders.

There is a good deal of freedom in the design of digital-filter hardware. First, there is the option of series or parallel arithmetic and second, there are many logic elements which, properly combined, will perform the functions of the basic filter-components.

In LSI implementations of small systems, parallel arithmetic is preferable. Thus, a third-order 12-bit filter would comprise thirty-six 1-bit delay elements, two 4-input 12-bit adders and seven 12-bit multipliers.

Shift-registers or flip-flops can be used as the delay-elements of the filter. Any flip-flop will serve the purpose, but D flip-flops offer the convenience of single-line inputs.

The organization of the Adders depends on the speed requirements. Ripple-propagation carry is acceptable in slow machines, but various look-ahead carry-propagation schemes (F3) are employed in

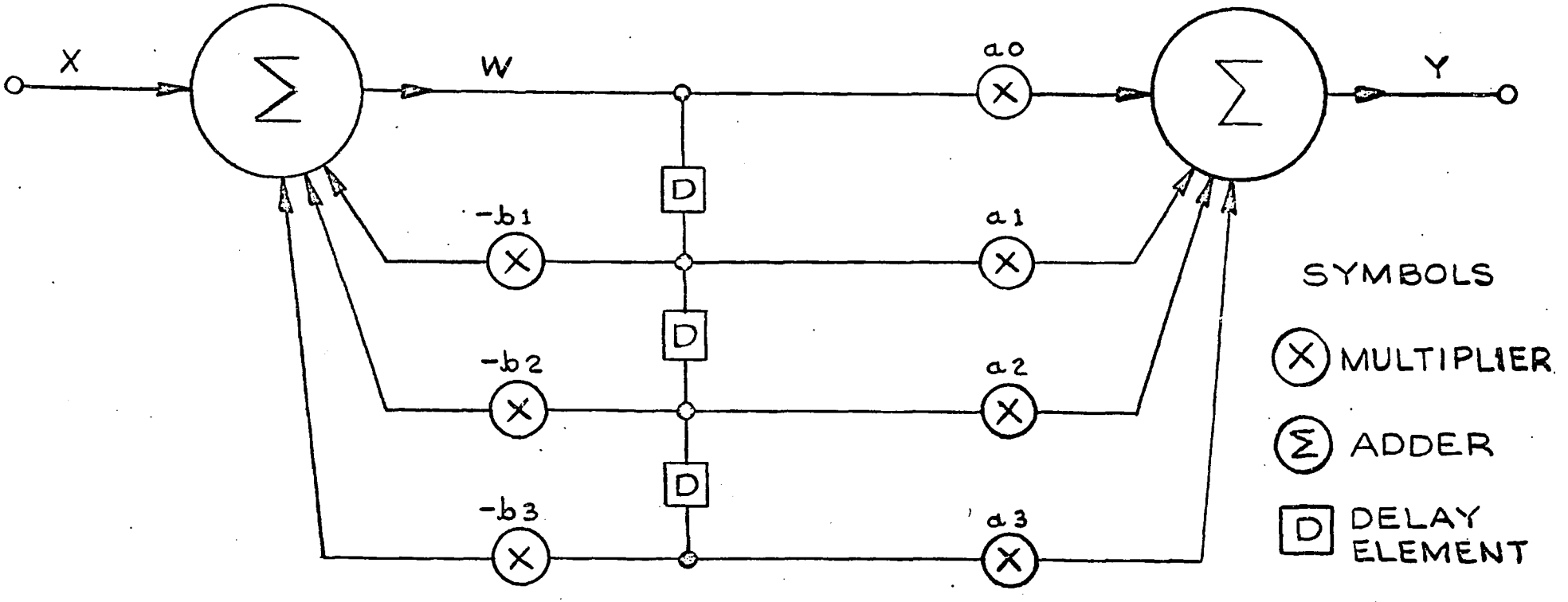


FIG.IV.2: TRIPLE POLE/ZERO DIGITAL FILTER

fast machines. Servo-control electronics generally fall into the former category; ripple-propagation carry should, therefore, suffice.

Multipliers are the most critical components of digital filters. They determine the versatility of the entire filter. Note that the configuration of the filter (Figure IV.2) is independent of the coefficients of the transfer function; it depends only on the order of the transfer function. The coefficients show up in the Multipliers and nowhere else.

It may be advisable to elaborate on this statement with regard to the order of the transfer function. To realize a third order function, we need three Delay-Elements, but a second order function can be generated by the same filter, if we include "zero" among the possible values of a_3 and b_3. Thus an n-th order filter will take care of all transfer functions of order n and less than n.

The versatility of digital filters stands in vivid contrast to the restrictive nature of analog filters.

Appendix III demonstrates some of the limitations of analog implementations. Equations (14) and (17) of Appendix III state the realizability conditions imposed on the coefficients of the transfer function by the configuration of Figure 6. To be reasonably rigorous, we would have to go one step further and determine the Bode-Sensitivity (B8) as the dependent variable of the coefficients of the transfer function. Sensitivity is in fact one of the reasons

behind the demand for comparative evaluation of alternative realizations of transfer functions (Appendix III and references S5, S6).

Returning to the multipliers we observe that we want the product of a variable and a constant

$$u_i(n) = k_i w_i(n) \tag{6}$$

This operation could be easily performed by primitive logic or a few shift-registers in combination with an adder. However, when designing LSI electronics, we must attempt to retain the intrinsic versatility of the digital-filter concept, in order to comply with the mass-production requisites of our technology. We turn, therefore, to "Read-Only-Memories" (ROMs) for the implementation of multipliers.

The fabrication and the principle of operation of solid-state ROMs are discussed in references B11 and N1. These devices are produced in large quantities in the form of "master-dice." Some custom processing of the dice is necessary, but its extent is limited to a metallization operation which determines the contents of the memory.

In our application, we use the independent variable $w_i(n)$ as the address and obtain the dependent variable $u_i(n)$ as the output of the memory. The constant multiplier k_i designates the contents of a given memory. Thus, in response to the address $w(n)$, a ROM labeled k_r will produce an output $k_r w(n)$ and a ROM labeled k_s will produce

the output $k_s w(n)$. To change the transfer function, we simply discard the old set of memories and insert a new one in its place.

The above discussion leads us into the topic of Adaptive-Filter hardware. Reverting to Figure II.5b, we consider the problem of modification of transfer functions under the control of commands from the central computer.

One solution is self-evident: we equip the filter with a few sets of memories and allow the computer to select the appropriate set.

Limited in scope as this method appears to be, it provides an answer to a real problem. As a missile moves through space its dynamics change because of variations in the density of the surrounding atmosphere and because of loss of balast due to expenditure of fuel. It is therefore necessary to have a repertoire of three or four transfer functions of the same basic structure, but slightly different coefficients. The selective-multiplier filter, proposed above, will provide these facilities.

The versatility of the adaptive process can be improved by a different realization of the multipliers. We consider the product

$$u_i(n) = k_i(n) w_i(n) \tag{7}$$

where $w_i(n)$ is the original multiplicand of equation (6), and $k_i(n)$ is a variable multiplier. To implement equation (7), we provide a compound multiplier to handle two variables and a Multiplier-Register

to store the number k_i. The contents of the Multiplier-Register can be updated by the central computer, when necessary.

Concluding this section, we observe once more the great versatility of digital-filters. The canonical filter configuration can be used for all rational transfer functions; implementation of adaptive filtration is equally simple.

The Digital Integrator

Our list of filter elements comprises three basic components, called the Adder, the Delay-Element and the Multiplier. It is expedient to add to this list one derived component, namely the Integrator.

To clarify the meaning of digital integration, let the level of data on a particular line be

$$f(0),\ f(1),\ f(2),\ \ldots\ldots\ldots f(n),\ \ldots\ldots\ldots \tag{8}$$

at instants

$$0,\quad 1,\quad 2,\ \ldots\ldots\ldots\ n,\ \ldots\ldots\ldots \tag{9}$$

Take a function g(n), such that

$$g(n-1) = f(0) + f(1)\ \ldots\ldots\ + f(n-1) \tag{10}$$

$$g(n) = f(0) + f(1)\ \ldots\ldots\ + f(n-1) + f(n) \tag{11}$$

$$g(n+1) = f(0) + f(1)\ \ldots\ldots\ + f(n-1) + f(n) + f(n+1) \tag{12}$$

The function g(n), defined by equation (11), is the digital integral of the sequence f(n).

To attain some proficiency in the manipulation of the digital integral, we refer to Figure IV.3 and write the sequence f(n) as

$$f(n) = f(t)\delta(t) + f(t)\delta(t-1) + \ldots f(t)\delta(t-m) \ldots \tag{13}$$

where:

$\delta(t)$ = Dirac's delta-function.

Equation (13) is equivalent to the expression:

$$f(n) = f(0)\delta(t) + f(1)\delta(t-1) + \ldots f(m)\delta(t-m) \ldots \tag{14}$$

It is, therefore, evident that f(n-1) can be written as

$$f(n-1) = f(0)\delta(t-1) + f(1)\delta(t-2) \ldots + f(m-1)\delta(t-m) \ldots \tag{15}$$

$$= E^{-1}f(n) \tag{16}$$

where:

E^{-1} = The Delay-Operator

In all of the above operations we have tacitly assumed that f(n) is equal to zero at negative values of t. We will obviously design our hardware to behave accordingly; philosophical niceties do not enter into the argument.

The transfer function, H(n), of the integrator can be obtained by subtraction of equation (10) from equation (11):

$$g(n) - g(n-1) = f(n) \tag{17a}$$

or, in accordance with equation (16),

$$g(n)(1 - E^{-1}) = f(n) \tag{17b}$$

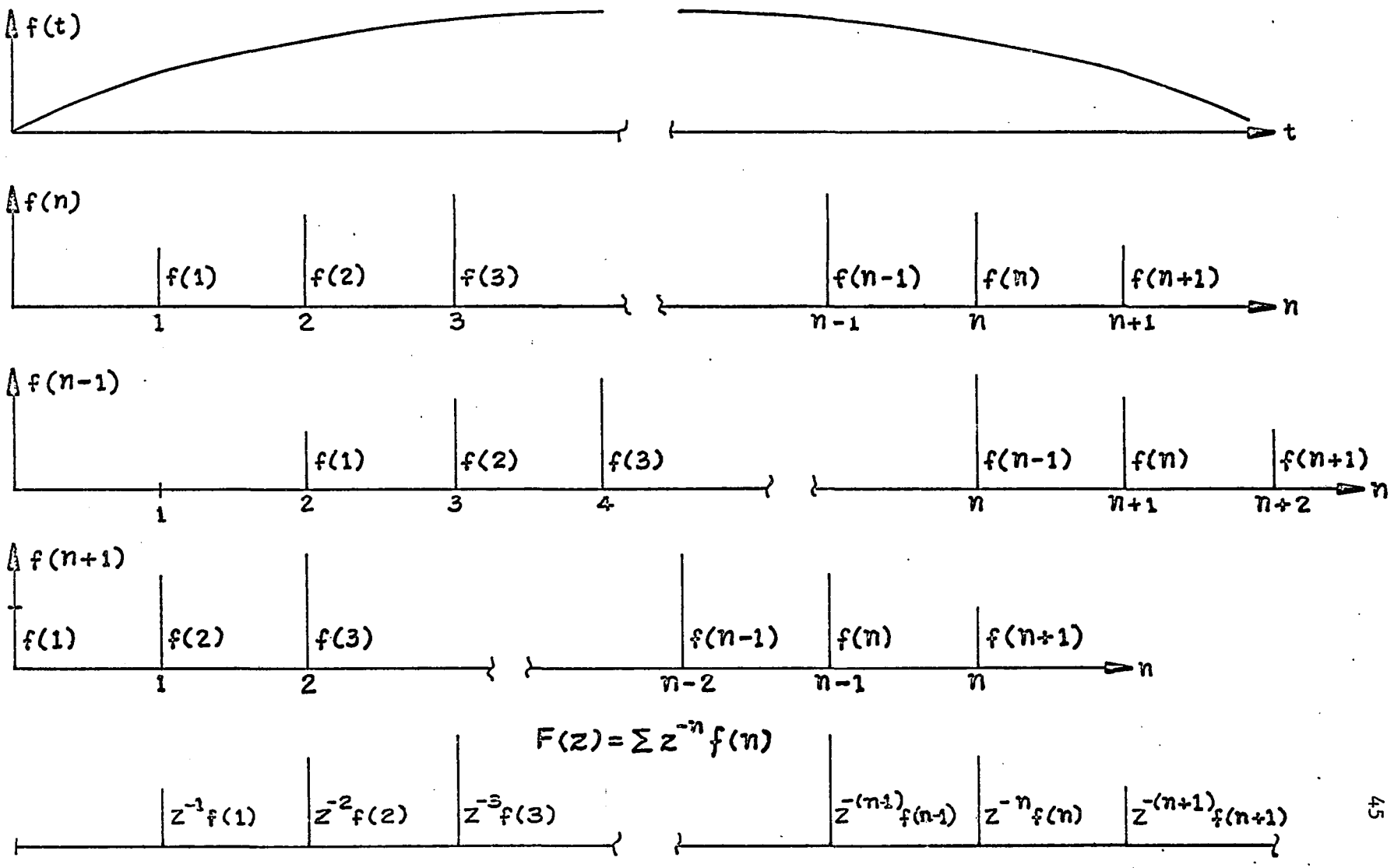


FIG.IV.3: SHIFTING OF A DISCRETE-TIME FUNCTION

Hence:

$$\frac{g(n)}{f(n)} = H(n) = \frac{1}{1 - E^{-1}} \tag{18}$$

Utilization of the digital integrator in function generators and frequency modulators will be demonstrated below.

The Z-Transform and the State-Space Representation

Mathematical details of the Z-transform are discussed in references L7, F4, A3 and practically all textbooks on transform calculus. For our purpose it is sufficient to associate the z-variable with the exponential of the Laplacian s-variable (e^{sT}). Let f(t) be a continuous well behaved function and let us expose it to uniform sampling. The sampled function f*(t) can be written as:

$$f^*(t) = \sum_{m=0}^{\infty} \int_0^{\infty} f(t)\delta(t - mT)dt \tag{19}$$

where:

$\delta(t)$ = Dirac's delta function

$1/T$ = Sampling rate

m = Integer

The Laplace transform of f*(t) is:

$$F(s) = \int_0^{\infty} f^*(t)e^{-st}\, dt \tag{20}$$

$$= \sum_{m=0}^{\infty} f(mT)e^{-smT} \tag{21}$$

Substitution "z" for "e^{sT}," we obtain the Z-transformation,

$$F(z) = \sum_{m=0}^{\infty} f(mT)z^{-m} \tag{22}$$

depicted in line 5 of Figure IV.3.

Of immediate interest in filter work is the transform of the delayed function f(t-T). By reference to line 3 of Figure IV.3 and the reasoning employed in the derivation of equation (16), we find that

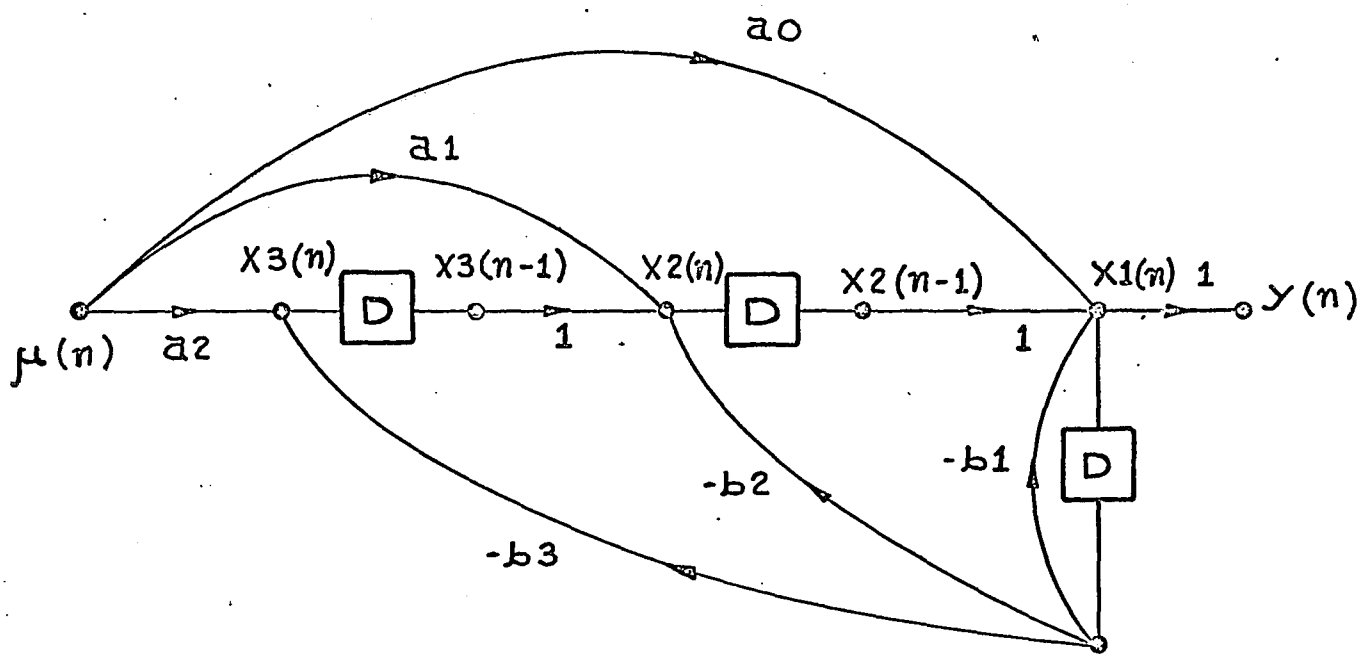
$$Z[f(t-T)] = z^{-1}F(z) \tag{23}$$

Comparing equation (23) with equation (16), we conclude that z^{-1} can be identified with E^{-1}, for the purpose of digital-filter synthesis.

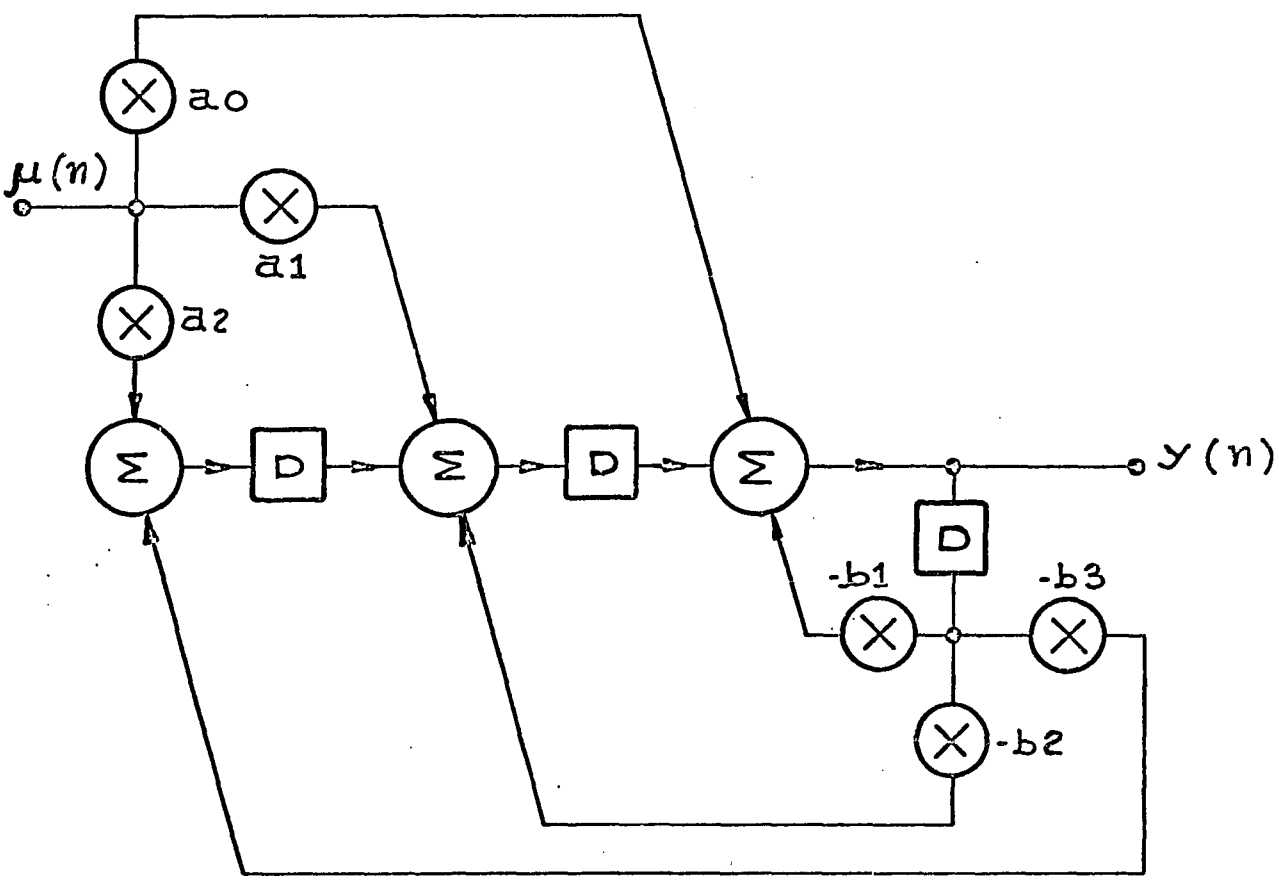
It does not make any difference whether a rational transfer function is written as $H(z^{-1})$ or $H(E^{-1})$; any set of components and any configuration which satisfies one of these expressions also satisfies the other.

Flow diagrams in State-Space variables differ from the corresponding block diagrams of digital filters only in symbolism and terminology. A weighted link in the former is a multiplier in the latter, while a node is equivalent to an adder and the delay-elements are the same in both interpretations.

Figure IV.4 shows the flow diagram and the schematic circuit of the equation:



a) FLOW DIAGRAM



b) COMPONENT DIAGRAM

FIG.IV.4: EQUATION V.25 IN STATE SPACE AND COMPONENT DIAGRAM REPRESENTATION

$$y(n) + b_1y(n - 1) + b_2y(n - 2) + b_3y(n - 3) =$$
$$= a_0u(n) + a_1u(n - 1) + a_2u(n - 2) \qquad (24)$$

State-Space interpretations are not unique. As with the previously discussed representations, there are many options. One convenient variation is shown in Figure IV.4. It is based on the following set of matrix equations:

$$\begin{bmatrix} x1(n) \\ x2(n) \\ x3(n) \end{bmatrix} = \begin{bmatrix} -b_1 & 1 & 0 \\ -b_2 & 0 & 1 \\ -b_3 & 0 & 0 \end{bmatrix} \begin{bmatrix} x1(n - 1) \\ x2(n - 1) \\ x3(n - 1) \end{bmatrix} + \begin{bmatrix} a_0 \\ a_1 \\ a_2 \end{bmatrix} u(n) \qquad (25)$$

$$y(n) = x1(n) \qquad (26)$$

Although one could standardize State-Space interpretations around Jordan's canonical matrices, no practical advantages would be derived therefrom. It is easier to transform from State-Space to a difference equation and then to the canonical filter of Figure IV.2.

Digital Differential Analyzer Implementations

Block diagrams of Digital Differential Analyzers (DDAs) resemble Analog Computer diagrams. DDA hardware resembles the digital filter components discussed in the preceding sections of this chapter.

Originally considered to be economical substitutes for regular digital computers, DDAs have been used occasionally as small, special-purpose machines. However, research-work in DDAs has been overshadowed by rapid progress in the development of conventional computers.

The emergence of the LSI technology will stimulate further development of DDA techniques. LSI facilitates decentralization of control-installations and generally favors small-system implementations. In their own right, DDAs have the advantage of compatability with Delta-Modulation (S8, P2, A1), which is increasingly used in aircraft navigation. Furthermore, they can be used to advantage in Kalman Filters, since they are very effective in the solution of linear and non-linear differential equations.

To illustrate the programming of DDAs, let us take Riccati's equation with constant coefficients:

$$y'' + ay' + by^2 = f(x) \tag{28}$$

Transformation of equation (28) into the form

$$d\left(\frac{dy}{dx}\right) = -a\left(\frac{dy}{dx}\right)dx - by^2dx + f(x)dx \tag{29}$$

explains the derivation of the block diagram of Figure IV.5a. Figure IV.5b depicts the same equation in the symbolism employed by Monroe (M9).

Monroe and other writers (M4, S8) use DDA blocks of one type only, while we employ the integrator and all basic digital-filter components. The former approach is directed at the user of DDA hardware; our method is clearer and more flexible from the standpoint of the designer of digital-filter components.

The application of Integrators to Pulse-Width-Frequency-Modulation is illustrated in Chapter V. The scaling and design of DDA systems is discussed in reference M4.

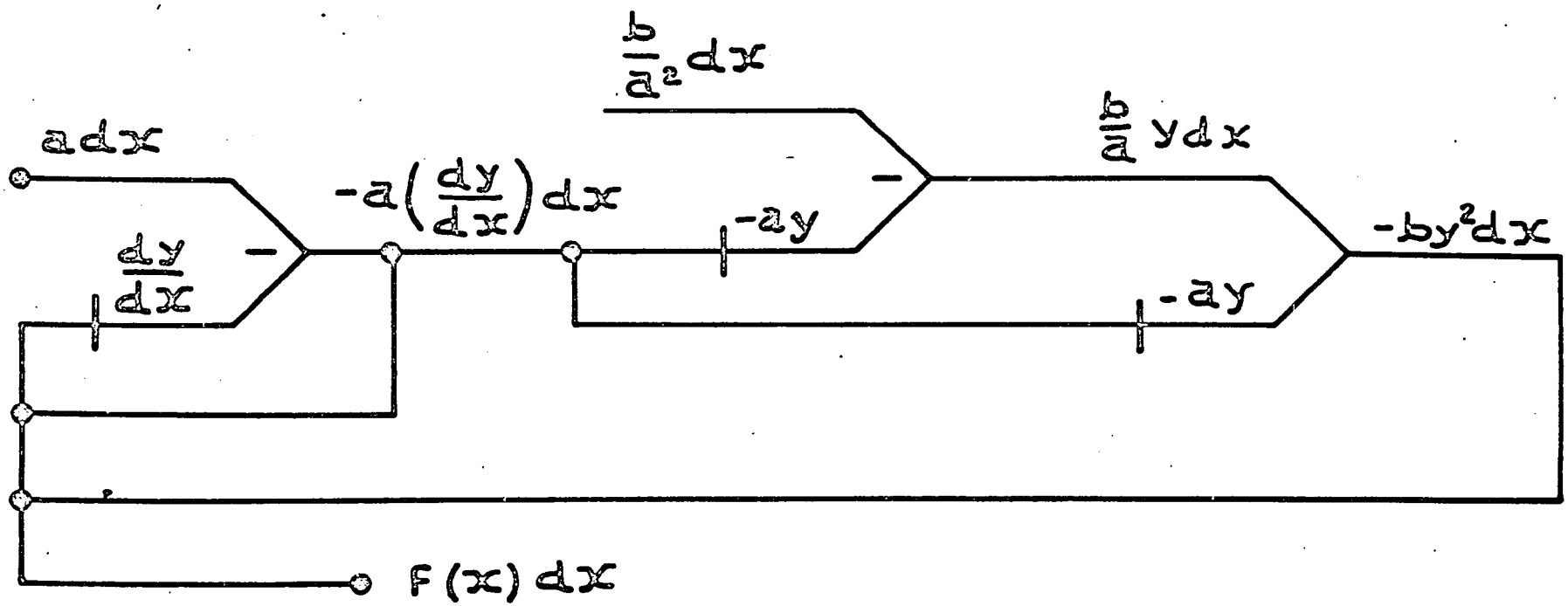


FIG.IV.5a: IMPLEMENTATION OF EQUATION IV.28

WITH DDA ELEMENTS.

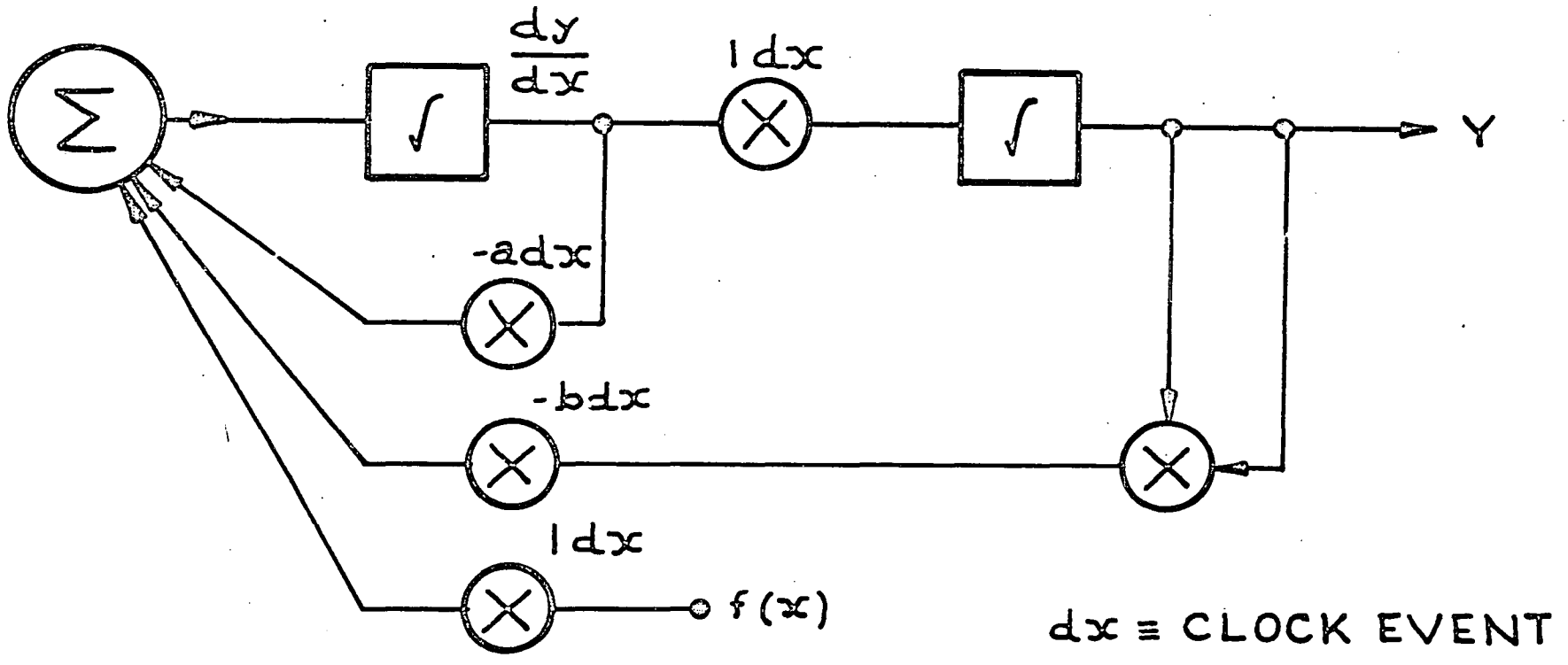


FIG.IV.5b: IMPLEMENTATION OF EQUATION 28

WITH STANDARD FILTER COMPONENTS.

Realization of Optimal Filters

The design of digital electronics generally allows for adequate margins against all reasonable noise phenomena. Nevertheless, some filtration may be necessary to cope with noise generated within the analog section (transducer) of a control system.

In simple cases, noise-effects can be taken into account in the design of the compensator. In complex cases, a separate module, designed around optimal-filtration principles, may be necessary.

Literature on optimal filters is still limited to computer algorithms for the optimization of stochastic data. This does not fulfill our requirements. We must go a step further in order to utilize LSI for the implementation of optimal filters. We will take, therefore, the best known filter algorithm (K1, H3, R5) and attempt to adapt it to our needs. We will examine Kalman's equations in order to: 1) reveal their physical meaning, 2) introduce some engineering simplifications and 3) justify the format of the covariance equation.

The following section is not self-contained. It should be read in conjunction with reference K1.

Kalman's filtering algorithm is derived in the fifth section (Solution of the Wiener Problem) of his paper.[1]

---

[1]R. E. Kalman, "A New Approach to Linear Filtering and Prediction Problems," ASME Transactions, vol. 82, part B, March 1960, pp. 35-45, Ref. K1.

He deals with a dynamic model described by the following set of discrete-time vector-equations:

$$x(t + 1) = \phi(t + 1;\ t)x(t) + u(t) \qquad K(16)$$

$$y(t) = M(t)x(t) \qquad K(17)$$

where:

$x(t)$ = State variables of random process (<u>unobservable</u>).

$y(t)$ = <u>Observable</u> random variables.

$\phi(t + s;\ t)$ = Transition matrix (<u>deterministic</u>).

$M(t)$ = Transformation matrix (<u>deterministic</u>).

The problem of Kalman's paper is formulated as follows: "Given the observed values of $y(t_0)$, ..., $y(t)$ find an estimate $x^*(t_1|t)$ of $x(t_1)$ which minimizes the expected loss."

A partial solution of the problem is given by equations (21) and (22) of the above reference:

$$x^*(t + 1|t) = \phi^*(t + 1;\ t)x^*(t|t - 1) - \Delta^*(t)y(t) \qquad K(21)$$

$$\phi^*(t + 1;t) = \phi(t + 1;\ t) - \Delta^*(t)M(t) \qquad K(22)$$

where Δ^* is a deterministic matrix which will be determined later.

Some insight into the meaning of the above two equations can be gained by combining them as follows:

$$x^*(t + 1|t) = \phi(t + 1;t)x^*(t|t - 1) + \Delta^*[y(t) - Mx^*(t|t - 1)] \qquad (30)$$

$$= \phi(t + 1;t)x^*(t|t - 1) + \Delta^*[y(t) - y^*(t|t - 1)] \qquad (31)$$

where:

$y^*(t|t - 1)$ = Predicted value of $y(t)$; an estimate based on the information available at $t - 1$.

Equation (31) shows that the estimate of $x(t + 1)$ is given by the sum of two terms. The first term,

$$u = \phi(t + 1;t)x^*(t|t - 1) \tag{32}$$

is the updated value of the previous best estimate, i.e. an estimate of $x(t + 1)$ based on information available at $t - 1$. The second term,

$$v = \Delta^*[y(t) - y^*(t|t - 1)] \tag{33}$$

is a correction deducted from the information which became available at event t. It is the weighted difference of the actual reading $y(t)$ and the projected reading $y^*(t|t - 1)$.

Equations (31) through (33) deserve some elaboration. Since the transition matrix $\phi(t + 1|t)$ is deterministic, we do not detract from the generality of the stochastic considerations by assumption of a unitary ϕ. We can then write

$$x^*(t + 1|t) = x^*(t|t - 1) + R[x(t) - x^*(t|t - 1)] \tag{34}$$

where: $R = \Delta^*M$.

Equation (34) tells us that the best estimate of $x(t + 1)$ after t observations is equal to the best estimate of $x(t)$ after $t - 1$ observations plus the weighted difference of the observed and estimated values of $x(t)$.

This is an intuitively obvious result. It resembles the conventional procedure for prediction of a stochastic variable on the basis of gradual influx of data. It is closely related to Bellman's Principle of Optimality and Swerling's approach to data-smoothing (S12). Equation (30) could be taken as the starting point of the derivation

of optimal filters. The essential problem is the derivation of the matrix Δ^*, regardless of the preliminary steps.

Returning to Kalman's paper, we note that

$$\tilde{x}(t + 1|t) = \phi^*\tilde{x}(t|t - 1) + u(t) \qquad K(23)$$

where:

$\tilde{x}(t_1|t)$ = Error in the optimal estimate of $x(t_1)$ at event time t.

$\phi^* = \phi - \Delta^* M$

The covariance matrix $P^*(t + 1)$ is defined as the expectation of the dot product of $\tilde{x}(t + 1|t)$:

$$P^*(t + 1) = E\tilde{x}(t + 1|t)\tilde{x}'(t + 1|t) \qquad (35)$$

where:

$E(x)$ = Expectation of x

x' = Transpose of x

Substitution of equation K(23) into equation (35) yields:

$$P^*(t + 1) = \phi^*(t + 1;t)P(t)\phi^{*\prime}(t + 1;t) + Q(t) \qquad (36)$$

where:

$Q(t) = Eu(t)u'(t)$

Kalman's result of the same operation is stated as:

$$P^*(t + 1) = \phi^*(t + 1;t)P(t)\phi'(t + 1;t) + Q(t) \qquad K(24)$$

Subtracting equation K(24) from (35), we obtain the difference V,

$$V = [\phi(t + 1;t) - \Delta^*(t)M(t)]M'(t)\Delta^{*\prime}(t) \qquad (37)$$

Since we cannot explain the above discrepancy with the available equations, we proceed to equation K(25) and the derivation of Δ^*.

Kalman obtains Δ^* from the orthogonality between $x(t + 1) - \Delta^*\tilde{y}(t|t - 1)$ and $\Delta^*\tilde{y}(t|t - 1)$, by writing:

$$E[x(t + 1) - \Delta^*\tilde{y}(t|t - 1)]\tilde{y}'(t|t - 1) = 0$$

He thus arrives at:

$$\Delta^*(t) = \phi(t + 1;t)P^*(t)M'(t)[M(t)P^*(t)M'(t)]^{-1} \qquad K(25)$$

Substitution of equation K(25) into (37) discloses the identity $V = 0$. One can, therefore, assume that Kalman tacitly anticipated equation K(25), in his derivation of $P^*(t + 1)$.

The optimal estimate of $x(t + 1)$ can now be expressed as follows:

$$x^*(t+1|t) = \phi(t+1;t)\{x^*(t|t-1) + R(t)[y(t) - M(t)x^*(t|t-1)]\} \qquad (37)$$

$$R(t) = P(t)M'(t)[M(t)P(t)M'(t)]^{-1} \qquad (38)$$

$$P(t+1) = \phi\{P(t) - R(t)M(t)P(t)\}\phi' + Q(t) \qquad (39)$$

The implementation of the above principles must necessarily depend on the complexity of the control installation.

Where there are many observables (y), co-ordination of operations by the Central Computer is necessary. Also, the solution of equations (37) through (39) is fairly complex (f1). One would, therefore, use the Central Computer for the execution of all calculations involved in the above Optimal-Estimate algorithm.

In self-contained loops, similar to those depicted by Figure II.4, there is only one observable. The matrix M(t) is, therefore,

a row-matrix and the product $M(t)P(t)M'(t)$ is a scalar. This simplifies equation (38) by elimination of the matrix inversion operation.

To detect further simplifications, note that although ϕ and P vary with time, they are not affected by the observable y. The covariance $P(t)$ depends only on time and $P(0)$, a pre-wired estimate of the initial errors. Note also that in practical cases M is a constant matrix, not $M(t)$ as generalized by Kalman.

Thus, it is feasible to use pre-calculated sequences of numbers for $\phi(t)$ as well as $P(t)$, if the asymptotic values of these quantities can be reached in a reasonable number of steps. A Read-Only-Memory, equipped with a program counter, will supply the necessary data at the appropriate time.

Where the dynamics of the system vary with time as described on page 42, different sets of memories can be selected by commands from the Central Computer.

Figure IV.6 depicts the implementation of the $x1(t + 1|t)$ component of a third order system. Quite a few elements are required. Discrete-transistor hardware would be awkward, but LSI implementations are easily realizable. Thus, single-observable Kalman filters can be implemented without recourse to central-computer calculations; LSI enables us to perform the pertinent operations in situ.

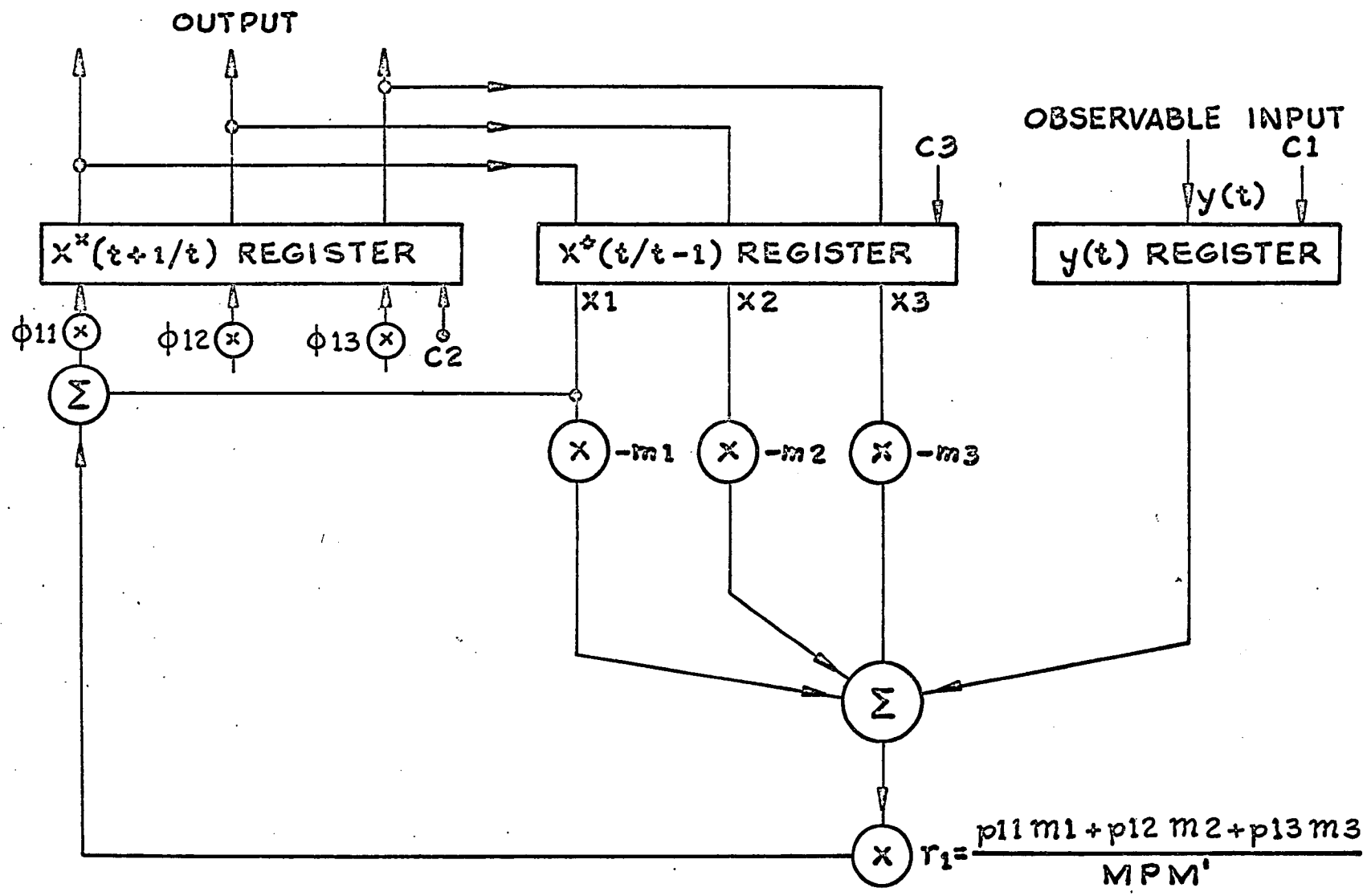


FIG.IV.6: IMPLEMENTATION OF EQUATION V.37

CHAPTER V

DRIVERS AND PULSE WIDTH-FREQUENCY MODULATION

Linearity and efficiency are important characteristics of power-drivers (W8). The linearity of the driver affects the dynamics and the accuracy of the entire system. Efficiency determines the excess power. Low efficiency calls for heat-dissipation accessories, while it imposes unwarranted demands on the batteries and other sources of energy.

Both of the above characteristics are particularly important in Aerospace applications. In a typical mission, the short-duration maneuver requirements are orders of magnitude higher than the prolonged stady-flight torquing-requirements.

In a discussion of efficiency (E), one must be guided by the overall efficiency ($\bar{E}$).

$$\bar{E} = (1/T) \int_0^T E[i(t)]dt \qquad (1)$$

where: $E[i(t)]$ = Efficiency as a function of load current,

T = Mission time,

or simply ask for high efficiency at all power levels.

Class B modulation is obsolete, by now, because it is inefficient at fractional loads. Modern systems employ Pulse-Frequency-Modulation (PFM) or Pulse-Width-Modulation (PWM). Analog versions of both techniques have been discussed in the literature. Reference M5

is a complete treatise on PFM systems, including analog to PFM conversion techniques of exceptional simplicity and elegance. Reference R7 provides some details of an Integrated-Circuit implementation of a PWM driver.

Our own interest lies in digital-input drivers. We present, therefore, all-digital versions of PWM and PFM and, subsequently, introduce the concept of Pulse-Width-Frequency-Modulation (PWFM), developed to overcome the limitations of the older techniques (see Figure V.1). Some component redundance is knowingly accepted, in order to simplify the explanation of PWFM.

Pulse Width Modulation

The transfer function of PWM can be expressed by the summation formula:

$$i(t) = \sum_{r=0}^{m} U(t - rT) - \sum_{r=0}^{n} U(t - rT - bT) \qquad (2)$$

where:

$U(t - rT)$ = Unit step at $t = rT$

T = Clock period

bT = Width of the output pulse = kp

p = Magnitude of the input quantity

k = Proportionality constant

$n = m - 1$ when $rT < t < (r + b)T$

$n = m$ $\quad (r + b)T < t < (r + 1)T$

Equation (2) displays the proportionality between the width of the

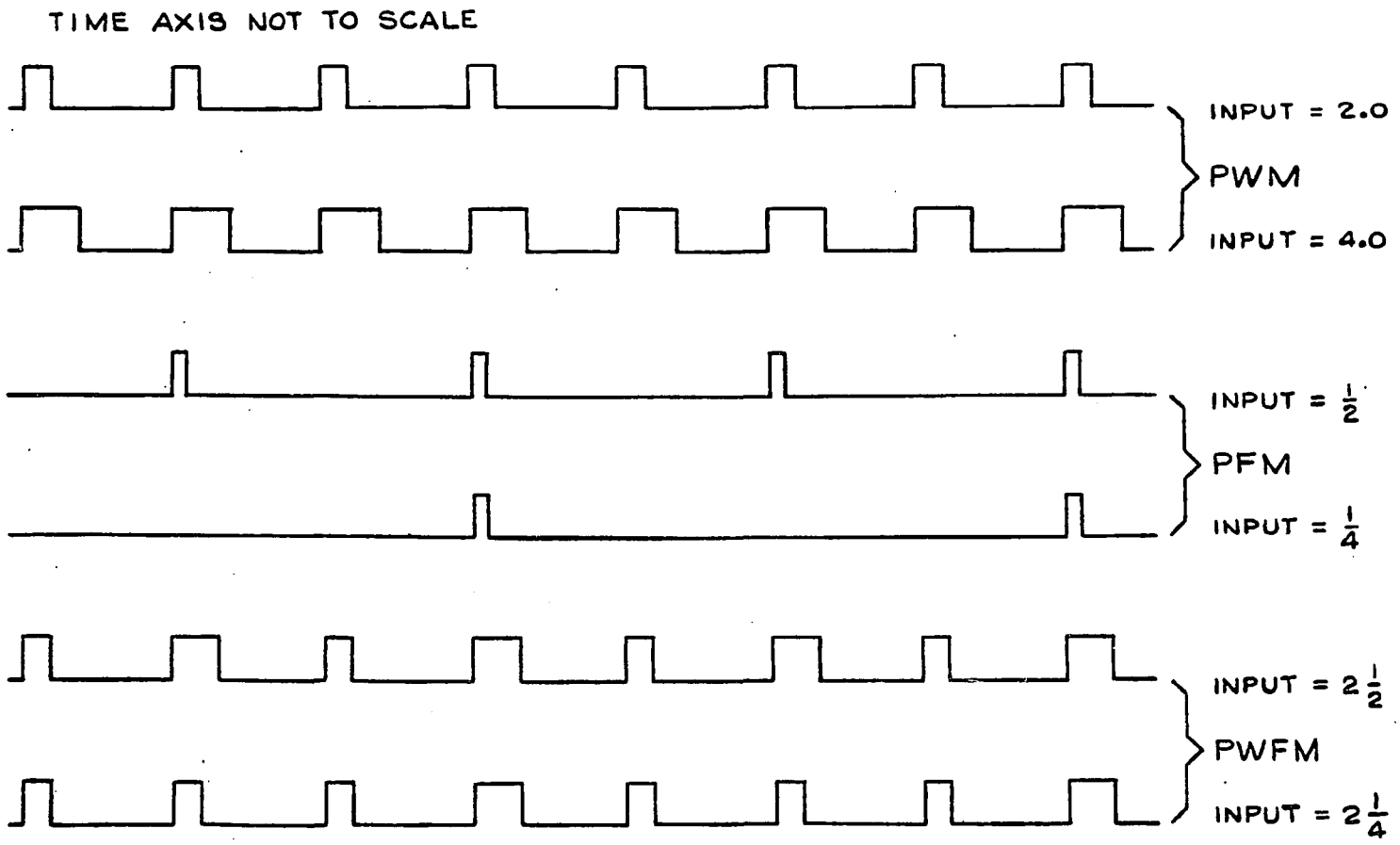


FIG.V.1: IDEALIZED RESPONSE OF PULSE MODULATORS.

output pulse and the magnitude of the input signal. Implementation of this principle is demonstrated in Figure V.2. The key-element of the basic width modulator is a 6-bit backward counter. The input gates (G1 through G6 and terminal D of FF1) accept a 7-bit word in sign-amplitude format (C8). Output pulses exit through one of two gates (G8 or G9), selected by the "sign" flip-flop FF1.

To examine the operation of the modulator, let a constant positive word of magnitude "p" be applied to the input gates. Also assume that gate G7 is initially in state zero and observe that the repetition rate of the triggers Tg1 and Tg2 is 64 times higher than the clock rate.

Begin with event C4(1), which sets the counter into state p (minterm of the counter equal to p), forcing gate G7 into state "one."

Trigger event Tg1(1) puts FF2 into state "one," marking the beginning of the output pulse and enabling input gate G10. The output pulse exits through gate G9.

Event Tg2(1) feeds a pulse into the counter, reducing its state to p - 1.

Tg2(2) sets the counter to p - 2, ... and so on, until event Tg2(p) finally brings the counter to state "zero," forcing G7 into state "zero."

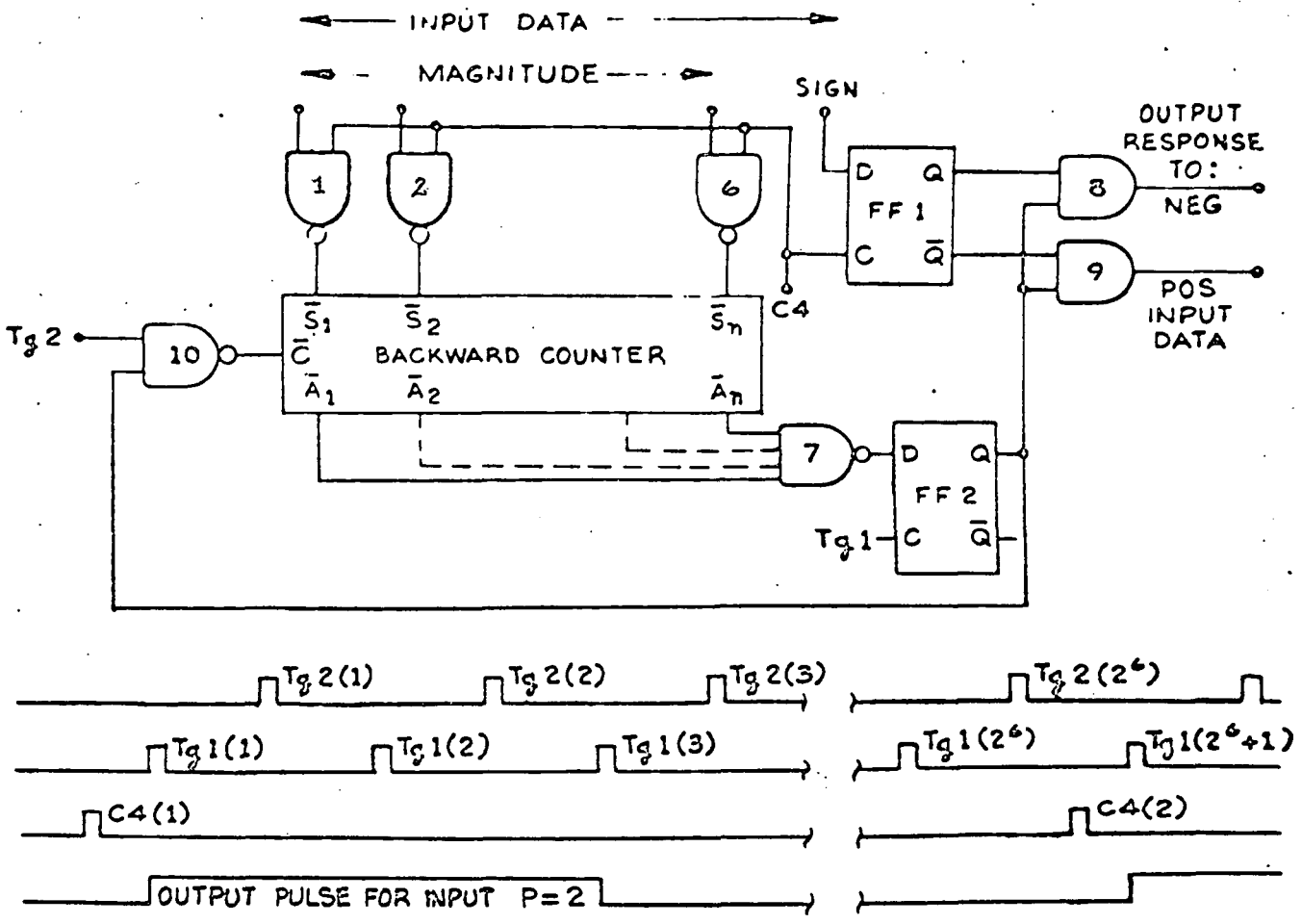


FIG.V.2: THE PULSE WIDTH MODULATOR.

Event Tg1(p + 1) resets FF2, terminating the output pulse and returning the modulator to the state assumed to exist prior to C4(1).

The next operational cycle begins at C4(2).

The above width modulator is only one of three elements of a typical power driver. To go from the modulator to the driver, we must add two peripheral units, as shown in Figure V.3: a format converter (Figure V.4) at the input and a power stage (Figure V.5) at the output end of the modulator.

The Format Converter

The purpose of the format converter is to reconcile the "two's complement" code of the compensator with the "sign magnitude" code required by the width modulator. In anticipation of PWFM, we assume a 12-bit input to the driver, although we dealt with a 6-bit modulator above.

The input word is divided into various subsets (Figure V.6) whose identity will be clarified as the argument develops. In the present context, the 5 least-significant bits (subset R) are used only for the purpose of proper conversion of negative numbers.

The logic-circuitry of the format converter operates in conformance with the following Boolean equations:

$$x = \prod_{j=0}^{5} \bar{A}_j \left(\sum_{j=6}^{11} A_j \right) \tag{3}$$

$$y_i = \bar{S}B_i + SD_i \tag{4}$$

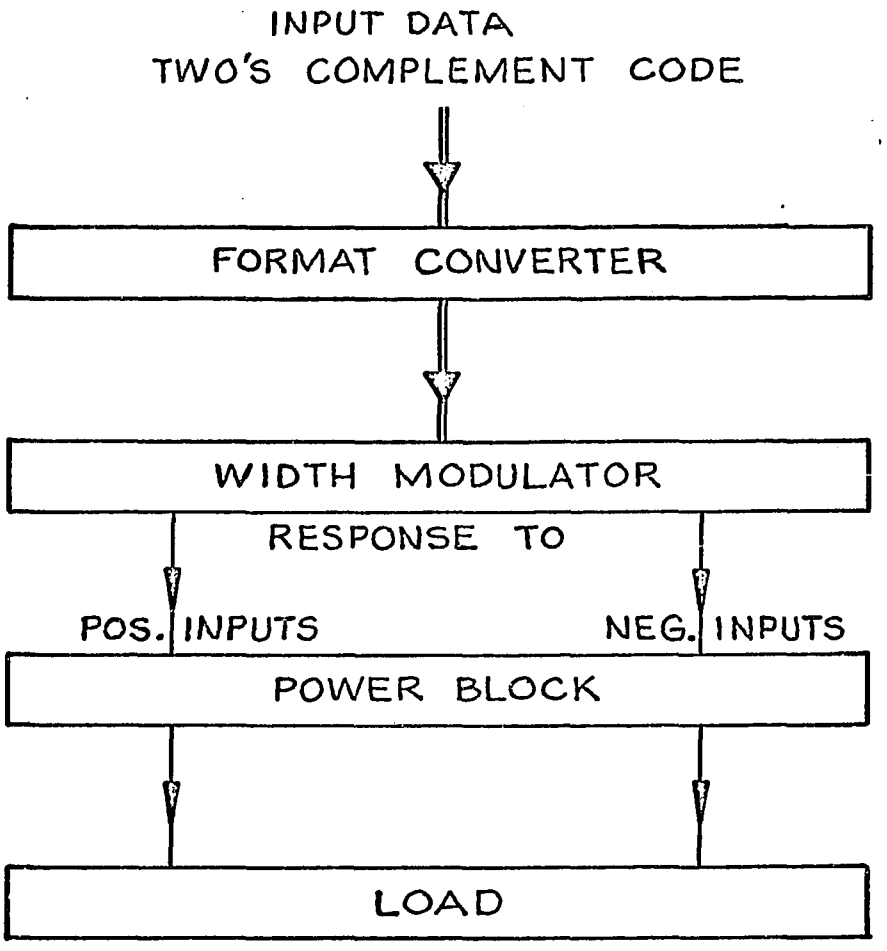


FIG.V.3: COMPLETE DRIVER

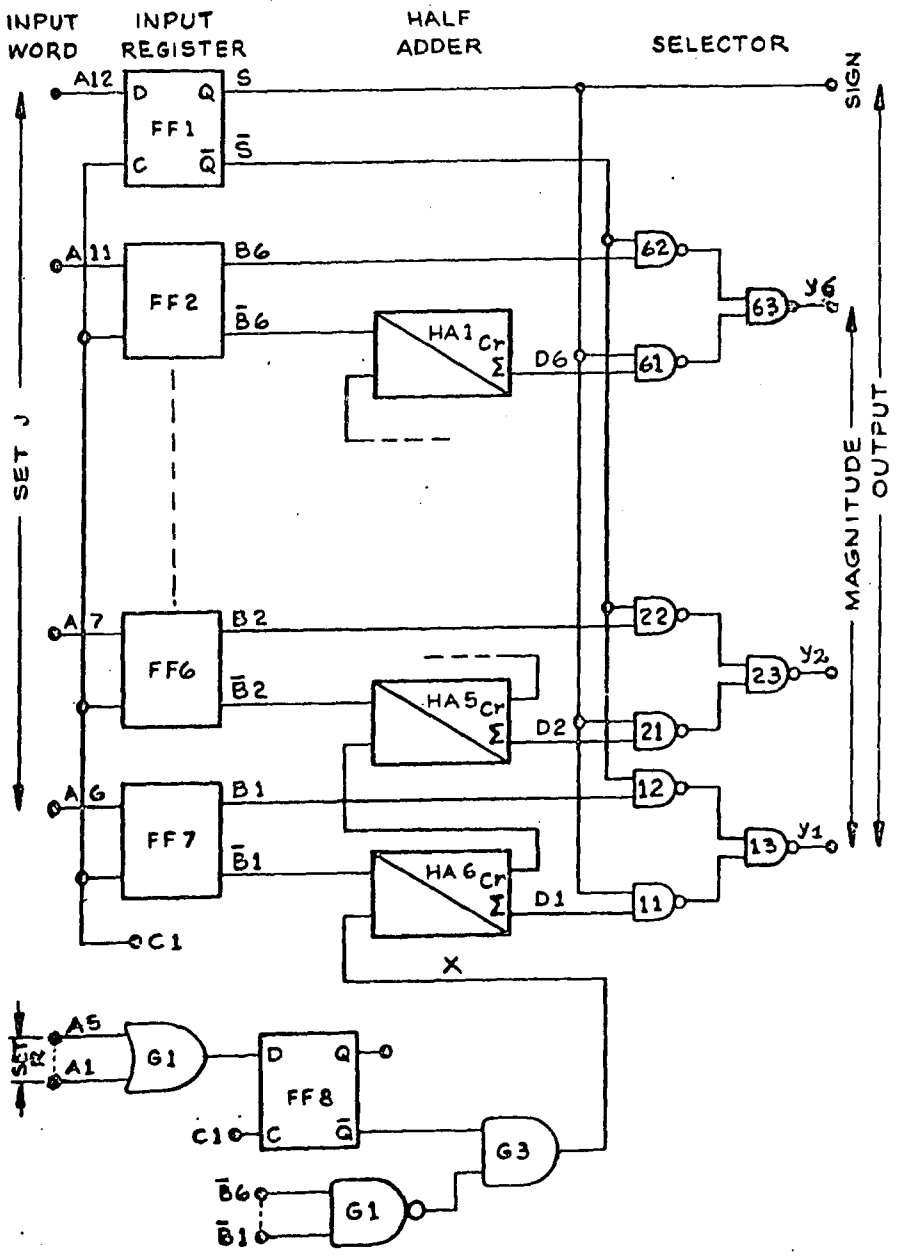


FIG.V.4: FORMAT CONVERTER

12-BIT TWO'S COMPLEMENT/7-BIT SIGN AMPLITUDE

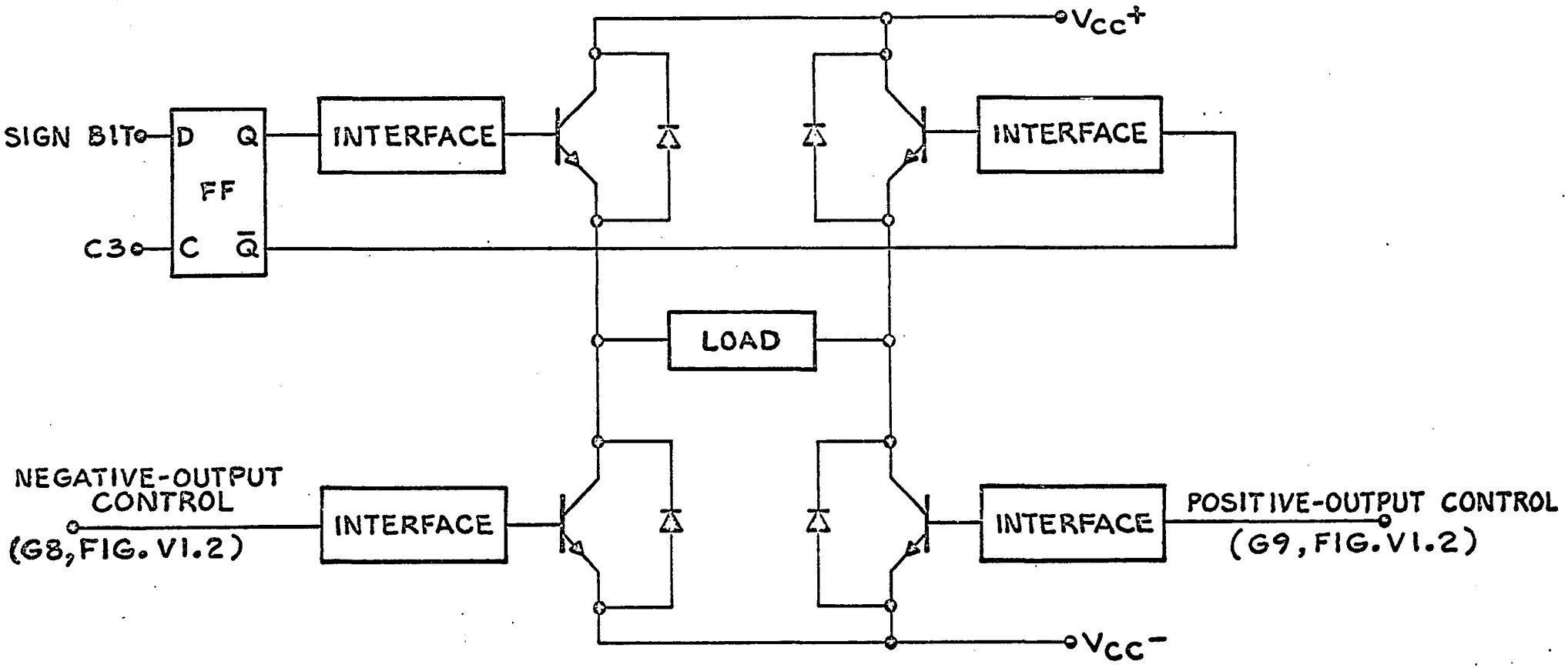


FIG. V.5: POWER STAGE

Pulse Frequency Modulation

Pulse Frequency Modulation (P2, M5) implies proportionality between the magnitude of an input quantity v(t) and the repetition rate f(t) of otherwise uniform output pulses. The output sequence, i(t), can be specified in terms of the Unit Step function U(t):

$$i(t) = \sum_{j=1}^{m} \delta_{mj}[U(t - \sum_{r=1}^{j} T_r) - U(t - x - \sum_{r=1}^{j} T_r)] \tag{5}$$

where: δ_{mj} = Kronecker delta

$T_r(t) = t_r - t_{r-1}$ = Spacing between consecutive pulses at $t = t_r$

x = Width of the pulse in seconds.

The delta function representation

$$i(t) = \int_0^{\infty} k \sum_{r=1}^{m} \delta(t - t_r)dt \tag{6}$$

is also legitimate, if its usage is restricted to frequency variation problems.

Analog Reset-Integrator implementations (M5) generally comply with the following equations:

$$f(t) = 1/T \tag{7}$$

$$\int_{t_{m-1}}^{t_m} v(t)dt = k, \text{ a constant} \tag{8}$$

$$t_m - t_{m-1} = T(t) \tag{9}$$

The proposed configuration of digital-input frequency modulators relies also on the principle of Reset-Integration, generally discussed in conjunction with Digital Differential Analyzers (M4, S8).

Before we examine the operation of the modulator, it should be stressed that we will use set H of Figure V.6 as the input signal. The six integer-order bits (set P) shall be disregarded in the following discussion of PFM.

Returning to set H, we refer to Figure V.7 which presents the block arrangement of the Reset-Integrator and to Figure V.8 which depicts the clock schedule of all Driver elements.

The input word is fed into the Increment-Register by clock C1, while the contents of the Transfer-Register are simultaneously but independently shifted to the Augend Register. The sum of the Increment and Augend words, formed in the Full-Adder block, is clocked into the Transfer-Register by event C2.

An overflow occurs whenever the above sum exceeds the capacity of the registers. This condition is detected by the gate complex G3 through G5, which performs the operation:

$$x = AB\bar{D} + \bar{A}\bar{B}D, \tag{10}$$

The output of G5 is clocked into the Overflow Flip-Flop at clock time C3. Gates G1 and G2 restore the sign-bit of the Transfer-Register to its proper value at C4, in accordance with the equations:

$$S = AB(C4)$$

$$R = \bar{A}\bar{B}(C4)$$

The polarity of the overflow can be taken from A or B, if required. It should be noted that the re-setting of the sign-bit does not

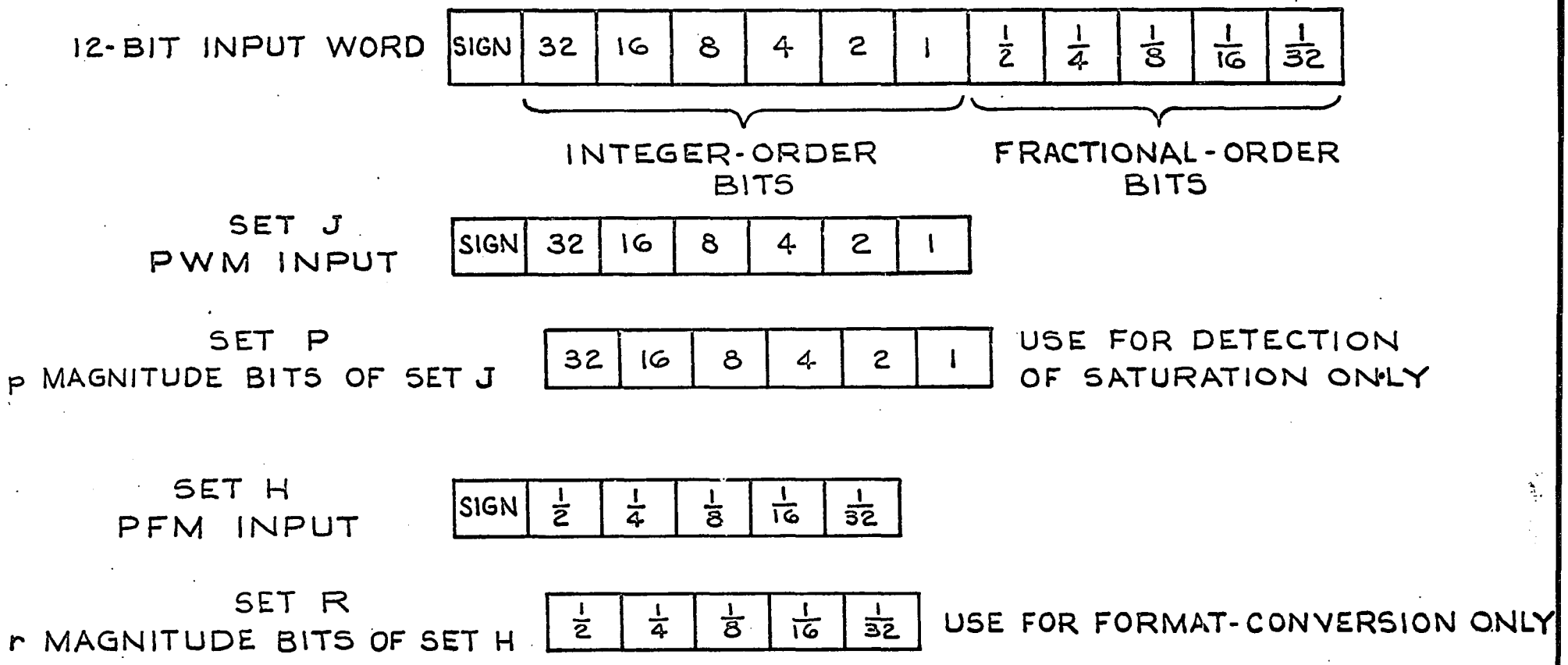
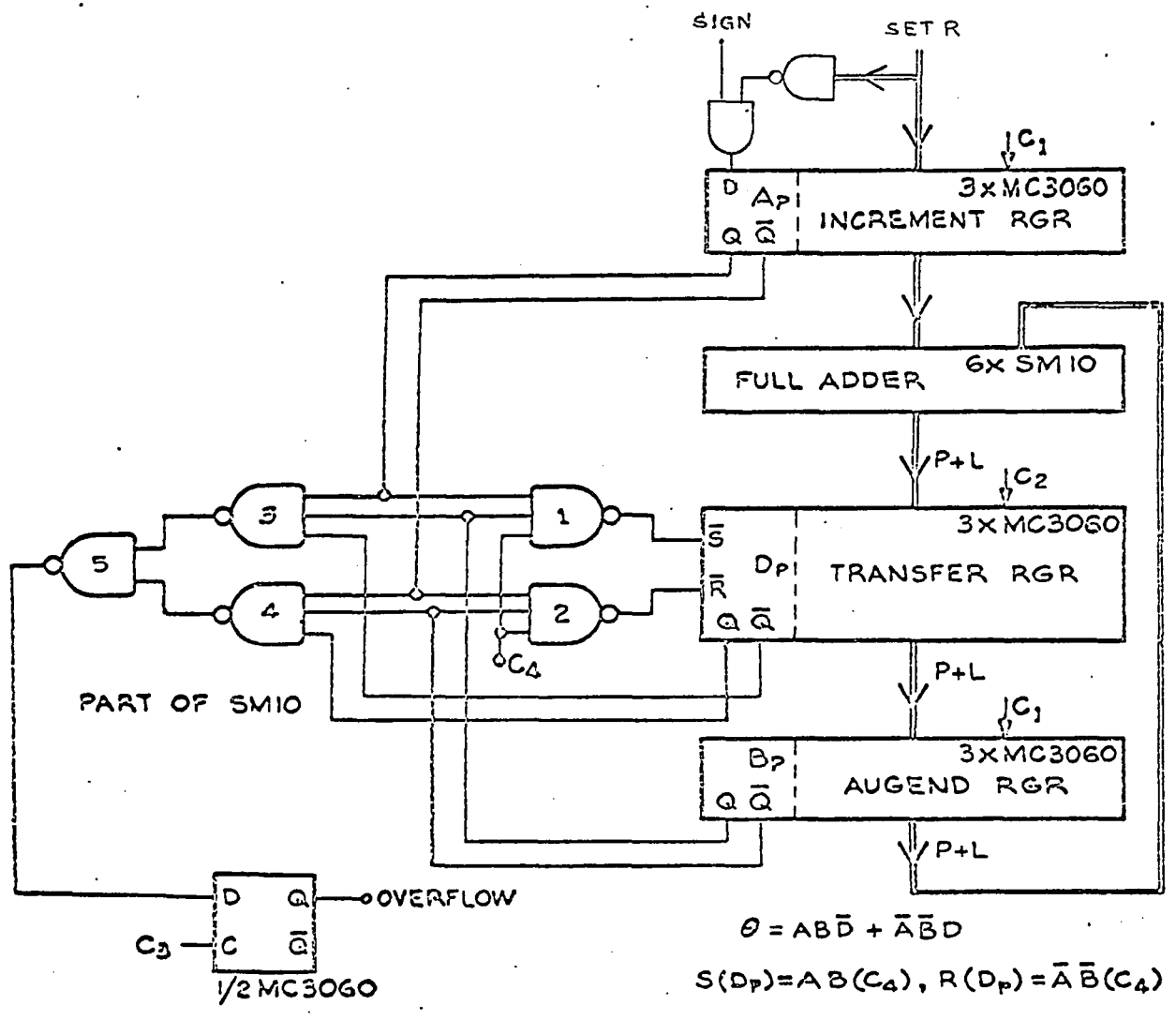


FIG. V.6: CLASSIFICATION OF INPUT-DATA INTO FUNCTIONAL SETS



$\theta = AB\bar{D} + \bar{A}\bar{B}D$

$S(D_P) = AB(C_4)$, $R(D_P) = \bar{A}\bar{B}(C_4)$

FIG.V.7: THE RESET INTEGRATOR.

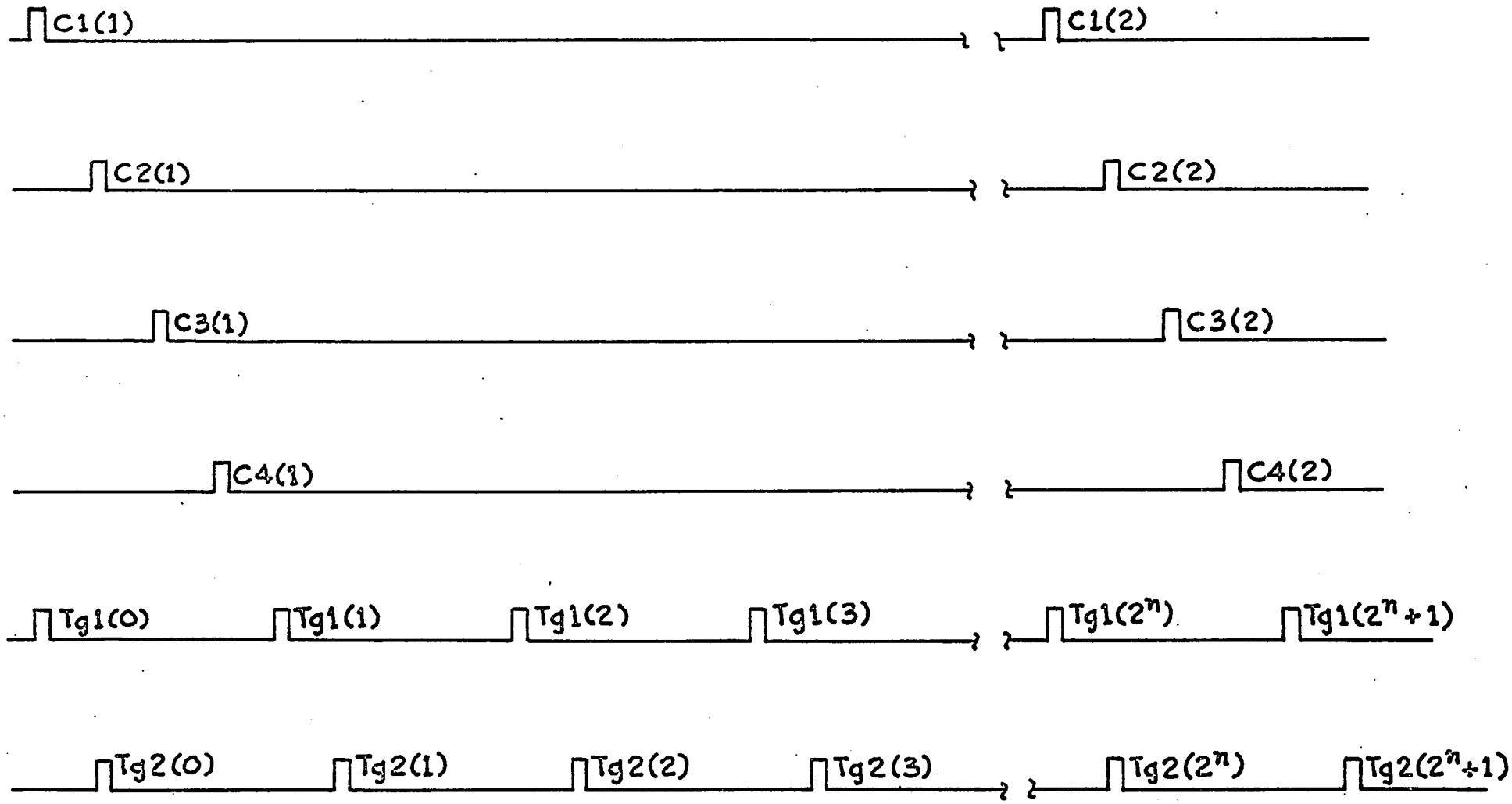


FIG. V.8: THE CLOCK SCHEDULE

affect the remaining 5 bits of the Transfer-Register. The Transfer-Register contains the correct remainder at all times.

The operation of the Reset Integrator can be further clarified by reference to Figures V.1 and V.9. At constant inputs, the modulator behaves like a frequency divider. Thus, with a fixed input of $1(2^{-r})$, the output sequence is:

$$\theta(t) = \int_0^\infty \sum_{k=0}^\infty \delta(t - kNT)dt \tag{12}$$

where: T = clock period

$N = 2^r$

$r + 1$ = Capacity of the Integrator, expressed in binary bits.

At inputs of $2^m(2^{-r})$, with $m < r$, equation (12) becomes:

$$\theta(t) = \int_0^\infty \sum_{k=0}^\infty \delta(t - kNT/2^m)dt \tag{13}$$

At inputs which are not expressible in simple powers of 2, some complications arise as a consequence of time and magnitude quantization. The response to step inputs, sometimes called the "Indicial Function" (G4), can be written as:

$$\theta(t) = \int_0^\infty \left[\sum_{k=0}^\infty (\delta_{x2})\delta(t - kNT - xT) \ldots + (\delta_{xi})\delta(t - kNT - xT) \ldots + (\delta_{xN})\delta(t - kNT - xT)\right] dt \tag{14}$$

$$= \int_0^\infty \sum_{k=0}^\infty \sum_{y=2}^N (\delta_{xy})\delta(t - kNT - xT)dt \tag{15}$$

where: (δ_{xy}) = Kronecker Delta

$\delta(t)$ = Dirac's Delta Function

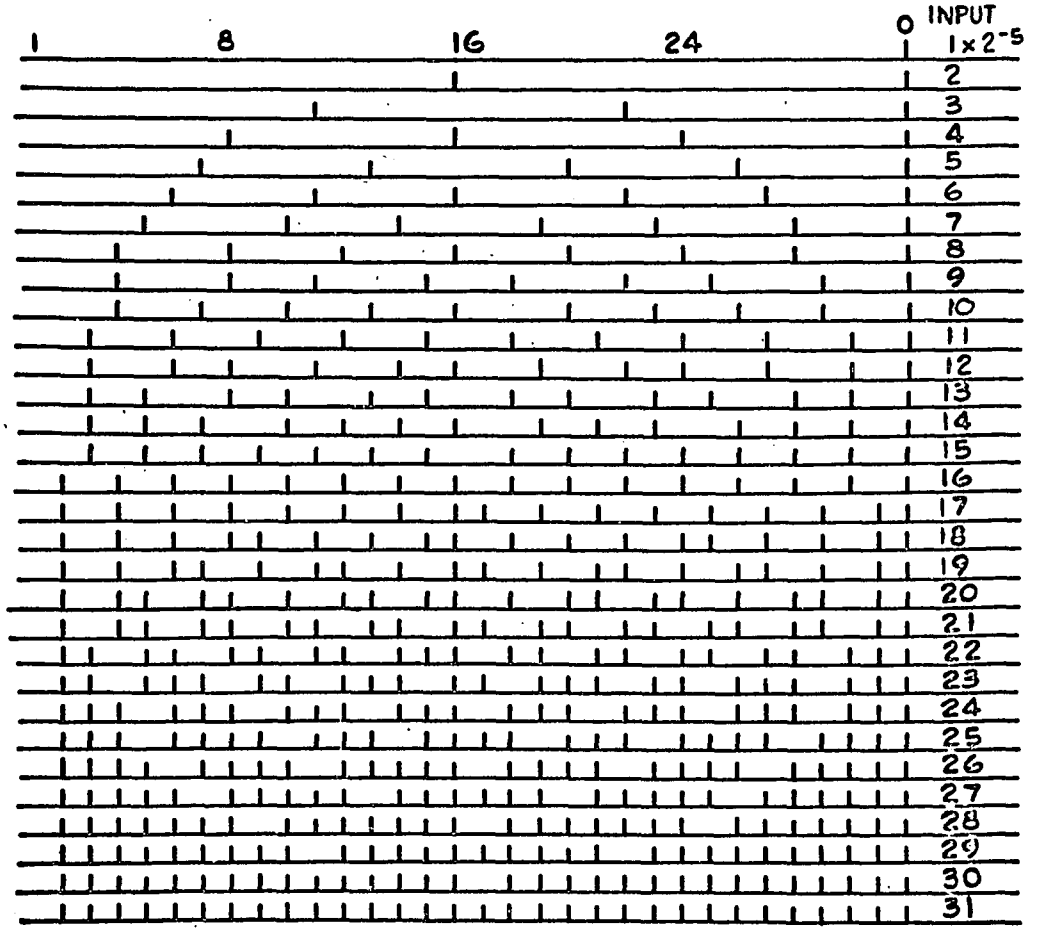


FIG.V.9: RESPONSE OF A 6-BIT RESET INTEGRATOR.

$x = y$ if $yi \geqslant mN$, while $(y - 1)i < mN$

$x \neq y$ in all other cases

i = Magnitude of the input signal, pre-multiplied by N.

k, y and m are integers.

It is apparent from equations (14) and (15) that the output sequence is periodic in the 2^r-th sub-harmonic with a period of $T_z = (2^r)T$.
The distribution of the pulses within the interval T_z may, however, be non-uniform to the extent of one bit (Figure V.9).

Representation of the indicial transfer function by a set of algebraic expressions is inconvenient from the point of view of analytic procedures. There are, however, a few extenuating factors. First, the format of equation (15) is entirely satisfactory for computer analysis purposes; Figure V.7 can be interpreted as an elementary form of a Reset-Integrator algorithm. Second, if the clock rate is sufficiently high, fractional width-bit interpretations are permissible. An output sequence of the form

0001000100010....

is then approximated by the fictitious sequence

$$\frac{1}{4}\ \frac{1}{4}\ \frac{1}{4}\ \frac{1}{4}\ \frac{1}{4}\ \frac{1}{4}\ \frac{1}{4}\ \frac{1}{4}\ \frac{1}{4}\ \frac{1}{4}\ \frac{1}{4}\ \frac{1}{4}\ \frac{1}{4}\ \ldots.$$

In principle, this procedure is always possible since, contrary to PWM practice, PWFM clocks can be run at almost arbitrarily high frequencies.

Deliberations on the topic of arithmetic representation of the Reset-Integrator response suggest a different implementation of this device.

Let us again consider the fractional-order input-set H, but with the assumption that it is in sign-amplitude format, not in two's-complement format. Treating the 5 magnitude bits as independent signals, let us feed them into a bank of individually weighted counters, as shown in Figure V.10. The 2^{-i} weighted bit is fed into an up-down counter, whose capacity is equal to 2^{+i}; algebraic accumulation of 2^i input pulses produces an overflow signal which is fed to the overflow register. All overflow lines are weighted at 2^0; the minterm of the summer is equal to $m_s = A + B + C + D + E$, in regular arithmetic notation.

Limitations of PWM and PFM

In principle, pulsed systems are 100% efficient. In practice, performance degradation shows up in the form of resistive losses and finite slewing. Both effects can be controlled, within reasonable limits, by device and circuit design. They are, however, interdependent and require different trade-offs for different applications. Device-wise, resistive losses depend on doping densities, horizontal geometry, vertical profile and metalization techniques. Storage phenomena and rise-time effects, evidenced as delays and deformations of the edges of the pulses, are controlled by the same factors, but in a different manner. Horizontal geometry creates the greatest conflicts in the design of fast, power switches.

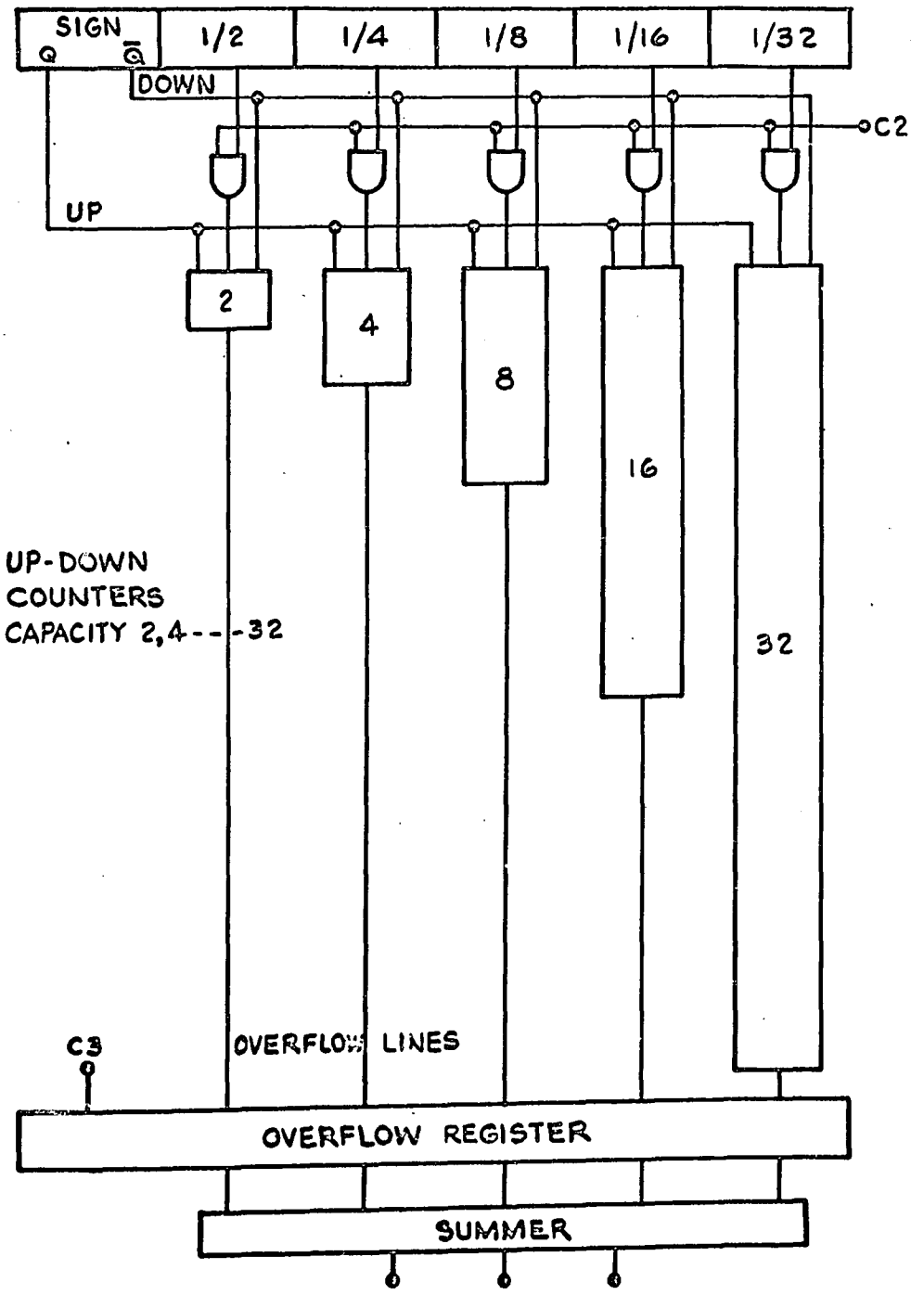


FIG.V.10: ALTERNATIVE IMPLEMENTATION

OF THE RESET INTEGRATOR.

Undesirable effects can be controlled to a certain extent by circuit-design measures, but compensation to better than 25% of the original error is unfeasible, because of fabrication tolerances.

There may also be applicational constraints on the maximum slewing rate of the output transistors, some imposed by EMI regulations, others by cross-talk precautions.

Our interest is confined to transient effects. We derive in Appendix I numerical expressions for the efficiency and linearity of pulsed drivers.

Omitting resistive losses and assuming the rhombic approximation of Figure V.11, the efficiency E works out to be

$$E = \frac{1 - 2T_r/3bT_o + T_f/3bT_o}{1 - T_r/2bT_o + T_f/2bT_o} \tag{16}$$

where:

bT_o = Width of the control pulse

T_r = Rise time of the output pulse

T_f = Fall time of the output pulse

$bT_o > T_r$

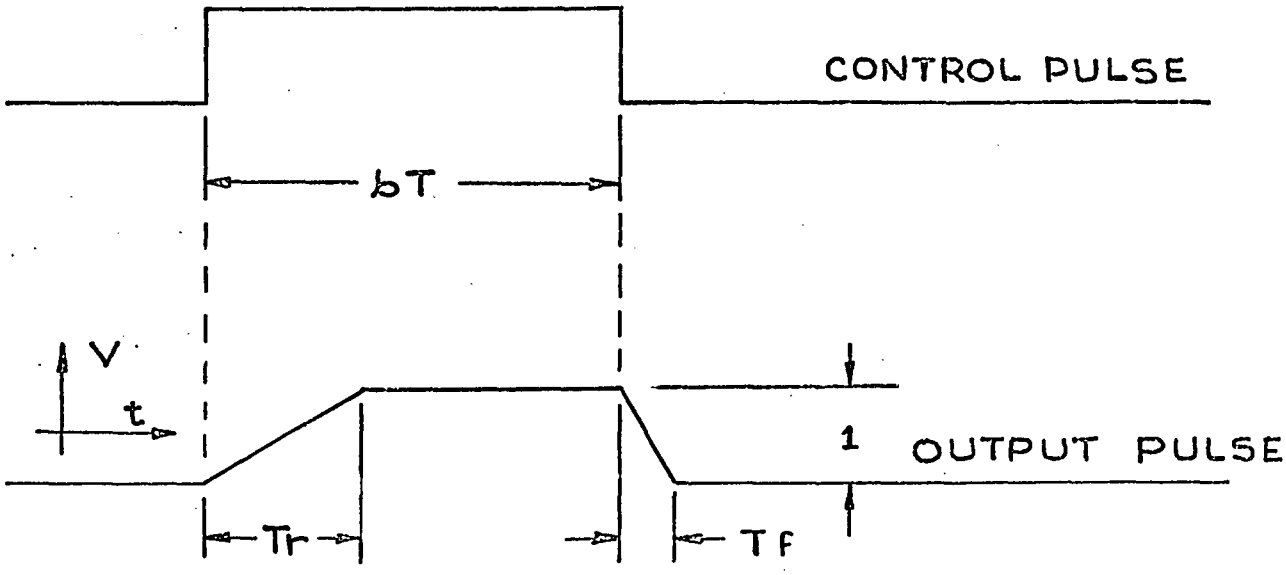
For pulse width shorter than T_r, or equal to T_r, the efficiency is 67%.

The linearity error is equal to

$$l_e = -\frac{1}{2}(T_r - T_f)/bT_o \tag{17}$$

when $bT_o > T_r$,

CASE 1: $bT \geq Tr$



CASE 2: $bT \leq Tr$

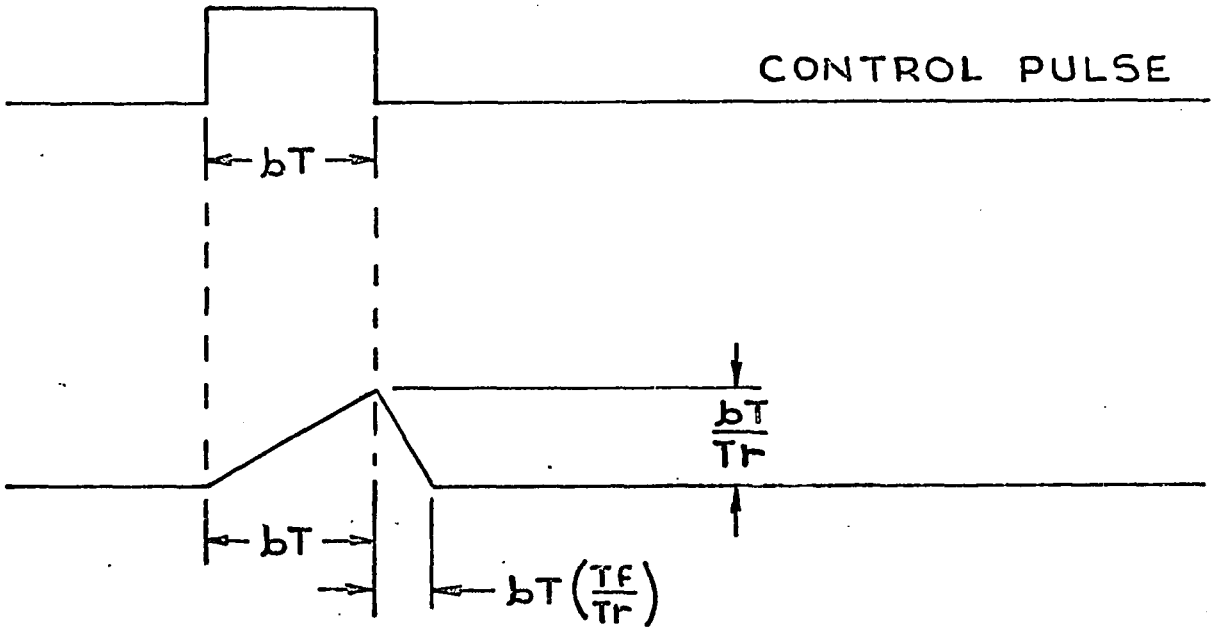


FIG. V.11: OUTPUT DISTORTION, RESISTIVE LOAD, RHOMBIC APPROXIMATION

and

$$l_e = 1 - \frac{1}{2}bT_o(1 + T_f/T_r)/T_r \tag{18}$$

when $bT_o < T_r$.

The term "linearity error," as used above, applies only to PWM. PFM systems are highly linear over the entire range of operations, especially at low signal levels. They are, however, relatively inefficient and suffer from severe power losses at high current levels. To improve efficiency, we must increase the basic output quantum; this is the main reason why PFM has been displaced by PWM in power-driver applications.

Speaking of PWM, we can reverse the above statement regarding efficiency and linearity. PWM is practically 100% efficient at high power levels but is very non-linear at low signal levels. This means that PWM has a badly restricted dynamic range. The linearity error is of the order of 25% at pulse widths (bT_o) comparable to the rise-time (T_r) of the output pulse.

In the system described by reference R7, the rise time is approximately .2 micro second. Operation at clock rates of 20 kHz. results in a linearity error of 10% at 1% and 87% at 0.1% of full output. This sounds well in general terms, but we must remember that Aerospace applications are somewhat unusual. Steady flight torquing is orders of magnitude below maneuver torquing. It is therefore necessary to maintain good linearity not only at 1% but also at 0.01% of full scale output.

We can improve the linearity of PWM drivers by reducing the clock-rate, but there are solid arguments against this trade-off. Operation at high clock rates reduces the delay indeterminance; it also simplifies supply-line decoupling, an important aspect of overall system engineering. Even more significant are the factors brought up in Appendix II, briefly outlined below.

Torquer coils are generally inductive, as the name implies. Therefore, some smoothing of the torquer current takes place automatically. The degree of smoothing depends on the clock-rate. The maximum ripple current (i_r) is given by equation (16), Appendix II, as

$$i_r = \tanh(gT/4)$$

where: $g = R/L = \dfrac{\text{Series resistance}}{\text{Series inductance}}$ of the torquer coil.

Thus, i_r can be reduced to 5% of the average current, if the clock rate is chosen to be 10 times higher than R/L. Equally interesting is the effective time constant (t_{ef}) of reactive loads under PWM excitation. By equation (26), Appendix II:

$$t_{ef} = (1/g) + (1/g)\ln. \frac{(e^{gbT} - 1)(1 - e^{-gT})}{bgT(e^{gT} - 1)}$$

where: bT = width of the pulse.

It reduces to L/R at clock rates in excess of 3R/L, an intuitively obvious result once it is stated.

Combining the remarks concerning equations (16) and (26) of Appendix II, we can state that, except for efficiency,

pulse-excitation of inductive loads at sufficiently high clock rates is equivalent to class A amplification, an important analytical and practical advantage.

Summarizing the advantages and limitations of pulsed systems, we conclude that a good servo driver should combine the efficiency of PWM with the linearity of PFM, while operating at relatively high frequencies. The concept of Pulse Width Frequency Modulation, described in the following section, has been developed by us to meet these requirements.

Pulse Width-Frequency Modulation

Having described all-digital versions of Pulse Width Modulation and Pulse Frequency Modulation we hardly need more than the principle of superposition to explain the concept of Pulse Width-Frequency Modulation. We recall that the input word was divided into various subsets (Figure V.6). Two of these are of immediate interest: subset J weighted in positive powers of 2 and subset H in negative powers of 2.

The somewhat unorthodox weighting scheme has been introduced for narrative purposes. Using it, we can say that PWFM responds to integer-order inputs in the width-modulation mode and to fractional-order inputs in the frequency-modulation mode. Integer-order inputs are fed directly to the basic width modulator, while fractional-order inputs are accumulated in the Reset Integrator until they add

up to unity and thus produce an overflow pulse which is subsequently summed with the prevailing integer-order input.

We turn now to Figure V.12, which shows a Reset Integrator tied into a width modulation system by means of a half-adder. Overflow pulses from the Integrator are fed into the half-adder at clock time C3, except when inhibited by gate G1. The latter event takes place only in case of saturation of the integer-order channel.

To follow the operation of the Pulse Width-Frequency Modulator, we assume that all registers are initially set to zero and we let the binary number

$$0000010,10000 = +2\frac{1}{2} \text{ (decimal)}$$

represent the input quantity.

Subset J, the most significant seven bits,

$$0000010 = +2 \text{ (decimal)}$$

enters the Augend ports of the Half-Adder at clock time C1(1), via the Format Converter.

Subset H, consisting of the five least significant bits and the sign bit,

$$0,10000 = +1/2 \text{ (decimal)}$$

is fed into the Reset Integrator, also at C1(1). At clock time C3(1), an overflow pulse from the Reset Integrator may appear at the Addend port of the Half-Adder. In the present instance the Overflow line remains at zero, since the total count in the Integrator is less

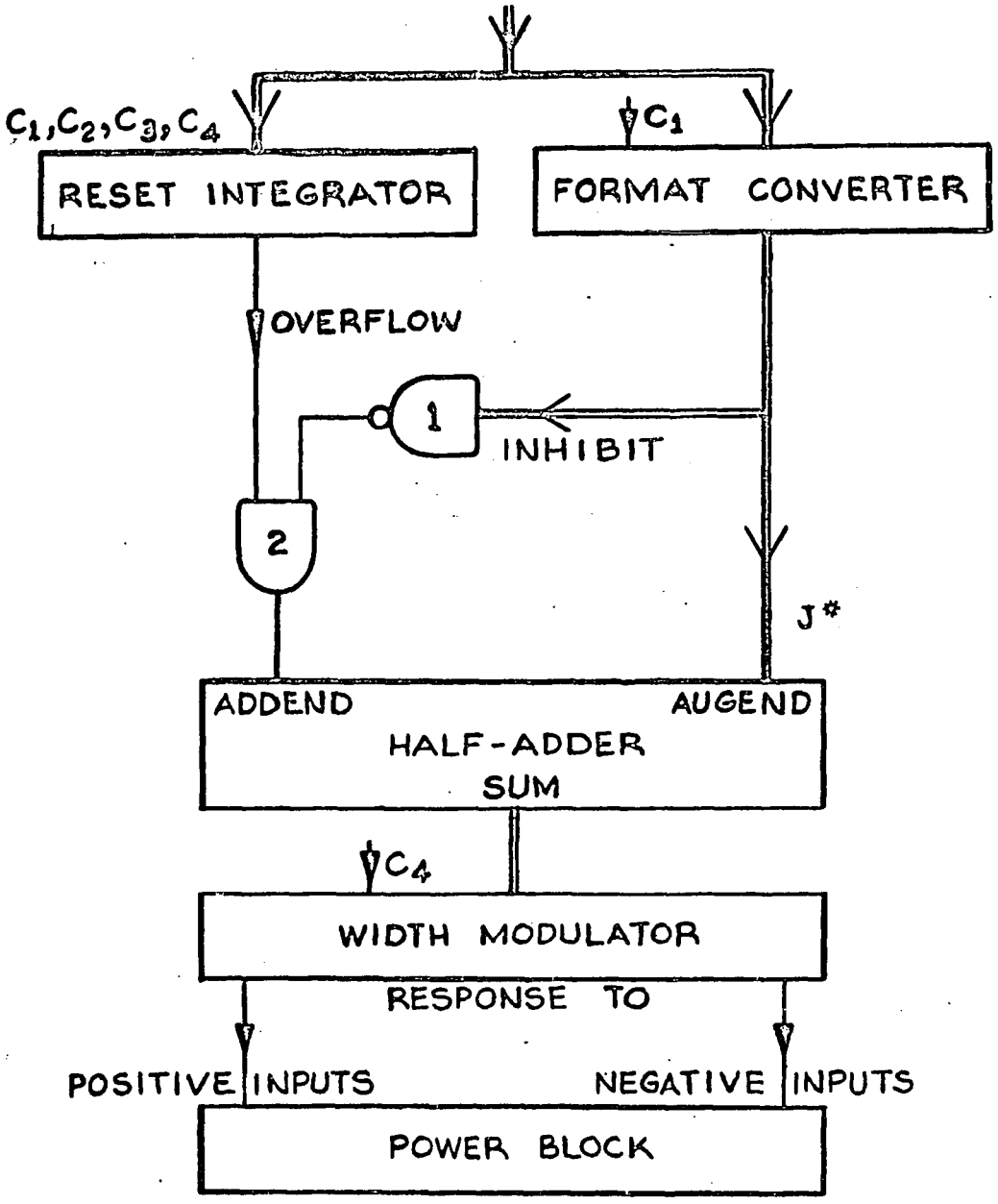


FIG.V.12: PWFM DRIVER

than one. Consequently, the input to the Basic Width Modulator at clock time C4(1) is

0000010 = +2(decimal).

It produces an output pulse of 2 width-units, one unit being equivalent to $1/2^6$ parts of the clock period. During the next operational cycle at time C1(2), the input registers are in the same state as they were at clock time C1(1). However, at C3(2), the overflow line is at "one," since the accumulated count is then equal to 1. Consequently, the input to the Basic Width Modulator is equal to 3 at C4(2), producing an output pulse of three units. During the third cycle a pulse of 2 width-units is again produced, followed by a pulse of 3 units during the fourth cycle. Thus, with an input of 2-1/2, the width of the output pulses alternates between 2 and 3 units (Figure V.1).

Incorporation of the second type of integrator (Figure V.10) into the Width-Modulation system is depicted in Figure V.13. It differs from the arrangement of Figure V.12 in three details: the Reset-Integrator is fed from the Format-Converter, the Saturation-Inhibit block is slightly more complicated and a Full-Adder is used to combine the WM and FM channels.

If we now represent a constant input signal by the equation

$$i(t) = \text{Sign},\ x_p 2^{p-1} + x_{p-1} 2^{p-2} \ldots + x_1 2^0 + x_{-1} 2^{-1} \ldots + x_{-r} 2^{-r}, \tag{19}$$

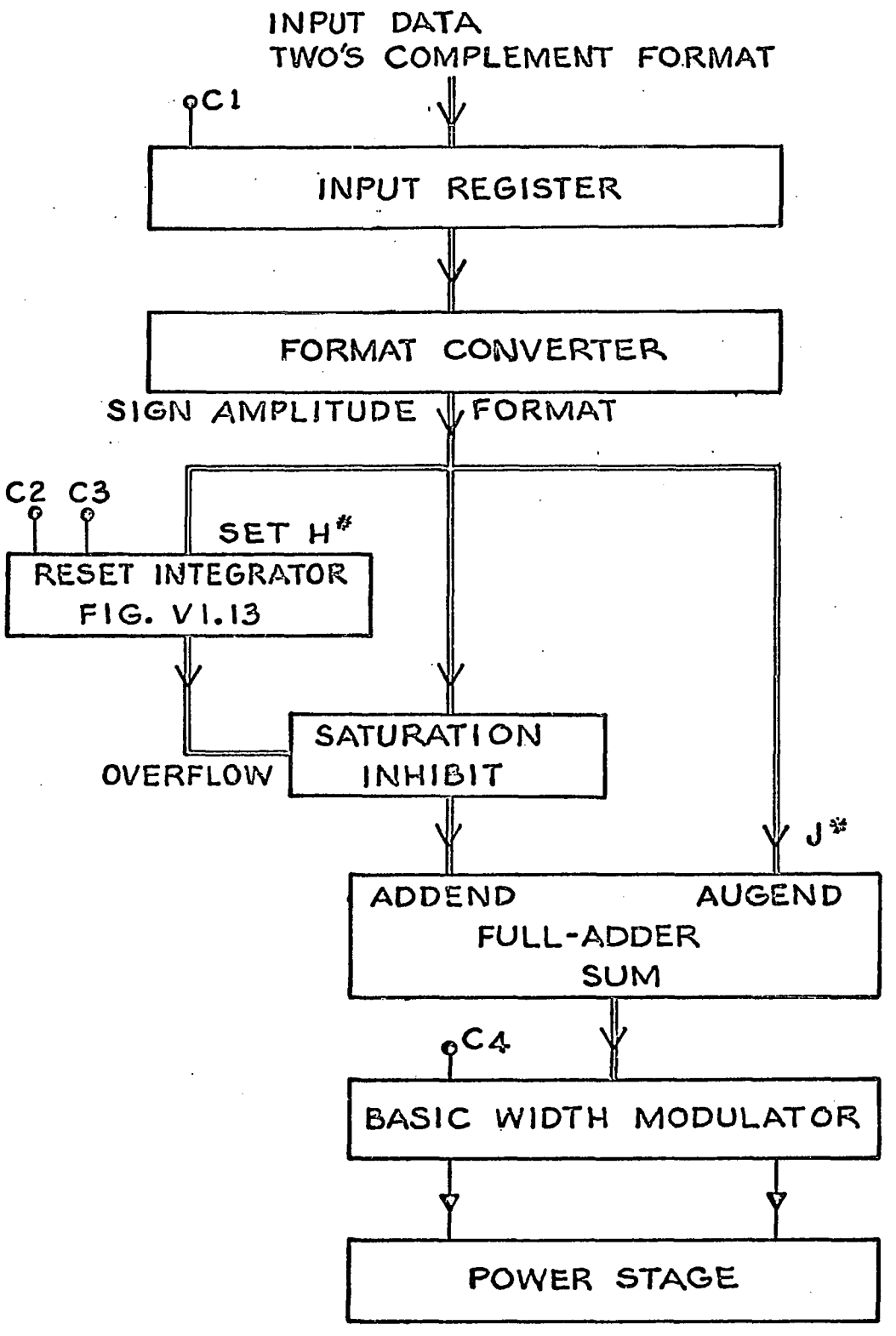


FIG. V.13: ALTERNATIVE IMPLEMENTATION OF A PWFM DRIVER

then we can write the output of the modified PWFM system as

$$\theta = \text{Sign}, (x_p 2^{p-1} + \ldots x_1 2^0)[\sum_{k=0}^{\infty} U(t - kT) - \sum_{k=0}^{\infty} U(t - kT - bT)]$$

$$+ x_{-1}[\sum_{k=0}^{\infty} U(t - 2kT) - \sum_{k=0}^{\infty} U(t - 2kT - bT)]$$

$$+ \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots$$

$$+ x_{-r}[\sum_{k=0}^{\infty} U(t - 2^r kT) - \sum_{k=0}^{\infty} U(t - 2^r kT - bT] \qquad (20)$$

At this stage of development of PWFM, the two implementations are considered to be comparible in merits and limitations.

To conclude this chapter let us examine the performance of an n-bit PWFM system operating at a clock-rate of 1/T seconds. Let

$n = 1 + p + r$

where:

p = # of magnitude-bits in the WM channel

r = # of magnitude-bits in the FM channel.

The basic pulse-width unit (w) is

$$w = T/2^p \text{ seconds.} \qquad (21)$$

The worst case linearity error (e_1) is

$$(e_1)_{max.} = 2^{p-1} T_r/T \qquad (22)$$

It sets-in at inputs equal to (2^{-p}) of full scale and remains constant down to zero-level signals. Thus, the dynamic range of the Basic Width Modulator is essentially infinite.

The dynamic range of a complete PWFM system is, of course, limited by the resolution of the input word (IR). This is equal to

the fractional value of the least significant bit. Thus,

$$\mathbb{R} = 2^{-(r+p)} \text{ of full scale,} \tag{23}$$

the standard quantization error of digital systems.

Efficiency, as interpreted in Appendix I, runs close to 100% at medium and high signal levels. It degrades slightly at low signal levels, the worst case being

$$E_{min.} = 1 - T_r/6w = 1 - 2P^{-1}T_r/3T \tag{24}$$

$$= 96\% \text{ when } p = 6,\ T = .2 \text{ micro sec.},\ 1/T = 20 \text{ kHz.}$$

To be realistic we must allow an extra 2% for resistive losses, and thus arrive at an overall efficiency of 94%.

This concludes the argument for PWFM, a modulation system characterized by good linearity and high efficiency. Operation at sufficiently high clock-frequencies results in performance equivalent to that of class A amplifiers. Implementation of PWFM is very simple, especially within the framework of digital servo-control electronics.

CONCLUSION

Approaching Servo-Control-Electronics from the extreme position of LSI for the sake of LSI, one would exclude analog implementations on the sole premise of storage-element requirements. Justifiable as this attitude might be, in the light of recent developments in the solid-state technology, it would detract from the strength of arguments based on the intrinsic advantages of digital techniques. These intrinsic advantages are as important as the indirect benefits which result from the LSI compatibility of digital circuits.

The past and present monopoly of analog techniques in servo-electronics is founded on traditional concepts of component economy. For every transistor in an analog circuit, we need at least 20 transistors in a comparable digital circuit. The LSI philosophy rejects the component-economy approach. We are allowed an almost arbitrary number of devices, provided that we use them in trouble-free circuit-configurations.

Revision of Sampled-Data electronics is long overdue. The designer may be restricted in the choice of hardware for the input side of the computer, but he has full control of the output hardware. Once the input information has been converted into digital format, there is no reason to convert back to analog; the computer can feed directly into a PW or PWF modulator. The power economy of pulsed drivers is advantageous in many applications. The ripple effects can be reduced to negligible proportions in all practical cases.

The mass-production character of the Silicon Technology is responsible for many of the complications encountered in the development of LSI servo-control electronics. Problems of centralization and standardization cannot be avoided. Standardization requisites are imposed by technological as well as economic factors.

At the circuit-fabrication level, we cannot limit ourselves to individual systems. Instead, we must evaluate the whole domain of servo-control applications and then design sets of different but compatible Detectors, Compensators and Drivers, to meet the demands of at least 60% of the total servo-electronics market.

Fortunately, digital systems are highly amenable to manipulations of scale factors. Provision of modular compatibility does not present any difficulty. The operating range of all modules proposed in Chapters III-V can be varied by adjustment of metallization masks alone.

Fringe benefits of digital techniques have been revealed by the discussion of organizational details of the proposed set of digital electronics.

The simplicity of computer-aided loops is remarkable. A standard Ratemeter feeds into the Central Computer which, in turn, activates a Width-Modulator. No peripheral hardware is required, conventional I/O facilities of the computer take care of all interface problems.

Implementation of certain adaptive-control schemes is equally simple. In stationary systems, the coefficients of the compensator (Figure IV.2) are fixed, and the multipliers perform the scaling operation

$$u_i = k_i x_i, \qquad k_i = \text{a constant.} \tag{1}$$

In adaptive control, the coefficients change with time and the multipliers perform proper multiplication

$$u_i = y_i x_i, \tag{2}$$

the variable y_i originating in the Central Computer.

Where the repertoire of y comprises but a few predetermined numbers, computer control of y can be exercised by selection of an appropriate Read-Only memory. Similarly, in Kalman filtration, a program counter can be used to align the components of the covariance matrix.

<u>Functional division</u> into operations performed by the Central Computer and operations performed by special purpose hardware depends on applicatory requirements. Autonomous loop organization should be used wherever specifications permit.

Where the operation of a particular loop is predicated on receipt of information from the Central Computer, the organization of the system is determined by the transmission rate of this information. If it is low, the adaptive-control configuration of Figure II.5b should suffice. If it is high, recourse must be taken to the arrangement of Figure II.5a.

Feasibility of digital techniques in servo electronics is demonstrated in Chapters III-V. Enough material is presented to reveal the intrinsic flexibility of the digital approach. Chapter V introduces the concept of Pulse-Width-Frequency Modulation. Circuit-level details are included in that chapter, in order to demonstrate the simplicity of PWFM hardware. The principle of PWFM is useful in applications which call for a combination of high efficiency and good linearity over a wide range of output power.

RECOMMENDATIONS

In our presentation of LSI electronics, we have proposed a few ideas related to the organization and implementation of functional modules for servo-control. A list of unsolved problems would be endless. Optimization of IC elements requires massive effort. It took five research teams, working continually since 1962, to bring the TTL gate to its present state of development.

Research-wise, analog implementations are still as important as digital implementations. Aging effects will be reduced sooner or later to acceptable proportions by improvements in passivation techniques. The capacitor problem is debatable. Capacitors are incompatible with LSI, but we continue to use them for line-decoupling purposes.

We will list, therefore, a few pressing problems in digital and analog microelectronics.

The Speed-Power Product is a perpetual problem, especially in Aerospace applications. We want higher speed and lower power dissipation, irrespective of the state of the art. This includes the performance of individual transistors, complete gates and complete subsystems.

The Threshold Level of logic gates is related to speed problems. Less swing means higher speed. The question is: how much, and what are the acceptable noise margins?

A V_{be} differential of 60 milli-Volts corresponds to current ratios of 10:1, yet commercially available gates are designed around noise-margins of about one Volt.

We must distinguish between internal gates and externally accessible gates of a system. Internal gates do not need the same noise protection as the external gates. It is therefore necessary to investigate the problem of trading noise margins against speed and power dissipation.

Digital filters, especially hardware implementations of digital filters require a good deal of research effort. Most of the papers which were published over the last few years dealt exclusively with the digitalization of analog filters and with computer algorithms of transfer-function equations. The emergence of LSI facilitates the implementation of small special-purpose machines, digital filters among them. This opens the question of optimization, including criteria of optimization. We are not greatly concerned with the total number of transistors or gates. The number of external terminals and cross-connections is far more significant; hence the importance of multi-function elements.

Stability of recursive implementations is a pressing problem. Stability of a difference equation does not imply stability of a filter which is subject to truncation errors. We are not necessarily interested in general solutions. Identification of configurations whose stability is insensitive to truncation errors is more important.

Kalman filters warrant a thorough engineering investigation. Their theoretical value is beyond dispute, but more research is required to determine their performance under practical conditions. The assumptions of white noise and predetermined noise power are highly speculative. In adaptive filtration, the effect of the rate of the noise variations should be further explored.

Structural simplifications of Kalman filters may be feasible. For example, where a fixed value of the initial covariance matrix is assumed, there is no need to perform the covariance calculations in situ; the results can be taken from a pre-wired memory. Furthermore, in some applications it may be permissible to work with the assymptotic values of the covariance matrix.

Digital Differential Analyzer realizations of servo-electronics deserve attention. The DDA principle provides easy means of implementation of regression equations. It can be used to advantage in Ratemeters and Filters; its utility in PFM and PWFM Drivers has been demonstrated in Chapter V.

It is advisable to revise the symbolism and the structure of the elementary DDA cell. Current practice in these matters, exemplified by references M9 and M4, is unnecessarily restrictive. The digital integrator, discussed in Chapter IV, is far more flexible, in our opinion.

Active RC Filters retain their importance and utility, in spite of current trends in technology.

One of the drawbacks of analog filters is illustrated by the material of Appendix III. The configuration of the filter depends not only on the order of the transfer function, but also on the magnitudes of its coefficients. It would be convenient, therefore, to have a computer program for the selection of feasible configurations of third and fourth order transfer functions.

A word of caution regarding over-simplification of the problem may be in order. A mathematician may claim that tandem arrangements of second order networks provide a "complete" solution of the compensator problem. This is a highly misleading statement from the point of view of engineering practice. Cross-cancellation of poles and zeros leads to gross errors and economic penalties. Performance criteria of active filters cover a number of factors which do not appear in the transfer function equation.

Noise effects in active filters require further research. For example, let us add another pole to equation (17) of Appendix III.

If we produce the extra pole at the input end of the amplifier, it will not attenuate the high-frequency noise of the amplifier. However, a low-pass network at the output end of the amplifier will attenuate the noise of the amplifier. The latter approach does not provide a practical answer; the complete solution of the problem may require considerable research effort.

Parasitic oscillations create the most pressing issue in all analog implementations, including active filters. Difficult as the

problem is, it can be solved by research in the area of device characterization. Currently used equivalent-circuit representation are too primitive to disclose the actual high-frequency performance of active devices. We need not be deterred by relatively complex representations. Appropriate computer programs will take care of the computational difficulties.

APPENDIX I

EFFICIENCY AND LINEARITY OF DIGITAL DRIVERS

The performance of pulsed drivers is degraded by resistive losses and various transient phenomena. Resistive losses show up as finite V_{ce} potentials across transistors connected in series with the load. They can be kept below 2% of the output power by appropriate circuit design methods. Transient effects induce delays and deform the edges of the output pulses. Delays can be controlled by various methods, but sloping of the edges of the pulses is a matter of basic device limitations.

Therefore, we will confine our attention to errors due to finite slewing of the output waves. Using the rhombic approximation of Figure V.11, we associate the slope of the leading edge with the rise-time T_r and the slope of the trailing edge with the fall-time T_f.

There are two possibilities: the control pulse may be longer or shorter than the rise-time of the output pulse. In the first case:

$$i(t) = t/T_r \qquad 0 < t < T_r \tag{1}$$

$$i(t) = 1 \qquad T_r < t < bT \tag{2}$$

$$i(t) = 1 - (t - bT)/T_f \qquad bT < t < bT + T_f \tag{3}$$

where:

$i(t)$ = Output current or voltage (Resistive load)

T = Clock period

bT = Width of the control pulse.

The integrated current (charge) per cycle is:

$$q = bT + T_f/2 - T_r/2 \tag{4}$$

while the energy per cycle (e) is:

$$e = bT + T_f/3 - 2T_r/3 \tag{5}$$

and the supply-line energy per cycle (s) is:

$$s = bT + T_f/2 - T_r/2 = q \tag{6}$$

We define the linearity error as

$$e_1 = (bT - q)/bT \tag{7}$$

It is therefore equal to

$$e_1 = 1/2(T_r/bT - T_f/bT). \tag{8}$$

The efficiency (E) is equal to the quotient of e over s,

$$E = \frac{bT + T_f/3 - 2T_r/3}{bT + T_f/2 - T_r/2} \tag{9}$$

The corresponding equations for the second case are:

$$q = (bT)^2(1 + T_f/T_r)/2T_r = s \tag{10}$$

$$e = (bT)^3(1 + T_f/T_r)/3T^2_r \tag{11}$$

$$e_1 = 1 - bT(1 + T_f/T_r)/2T_r \tag{12}$$

$$E = 2bT/3T_r$$

With resistive loads, the voltage rise-time is considerably longer than the fall time. We can, therefore, simplify the above equations as follows:

<u>Case 1</u>: $bT > T_r$

$$e_1 = T_r/2bT \tag{14}$$

$$E = \frac{1 - 2T_r/3bT}{1 - T_r/2bT} \tag{15}$$

<u>Case 2</u>: $bT < T_r$

$$e_1 = 1 - bT/2T_r \tag{16}$$

$$E = 2bT/3T_r \tag{17}$$

APPENDIX II

ANALYSIS OF PWM EXCITATION

The current in an inductive load under PWM excitation (Figure Appendix II.1) can be evaluated by means of the convolution integral:

$$i(t) = \int_0^t v(x)y(t - x)dx \tag{1}$$

where:

$$v(x) = \sum_{r=0}^{m} U(x - rT) - \sum_{r=0}^{n} U(x - bT - rT) \tag{2}$$

$$U(x - rT) = \text{Unit step at time } x = rT \tag{3}$$

$$n = m - 1, \text{ when } mT < x < (b + m)T \tag{4}$$

$$n = m, \text{ when } (b + m)T < x < (1 + m)T \tag{5}$$

$$y(x) = (1/L)\exp.(-gx) \tag{6}$$

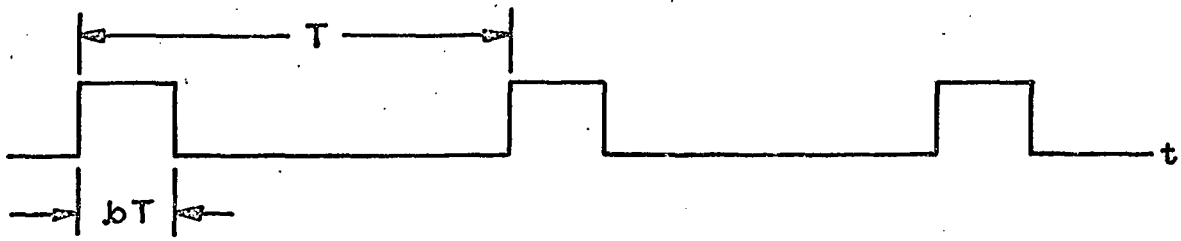
$$g = R/L = 1/T_1 \tag{7}$$

Substitution of equations (2) and (6) into (1) gives

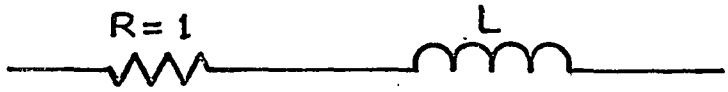
$$i(t) = \sum_{r=0}^{m} (1 - e^{-gt}e^{grT}) - \sum_{r=0}^{n} (1 - e^{-gt}e^{gbT}e^{grT}) \tag{8}$$

$$= m - n - (e^{-gt}) \frac{e^{g(m + 1)T} - 1 - e^{gbT}(e^{g(n + 1)T} - 1)}{e^{gT} - 1} \tag{9}$$

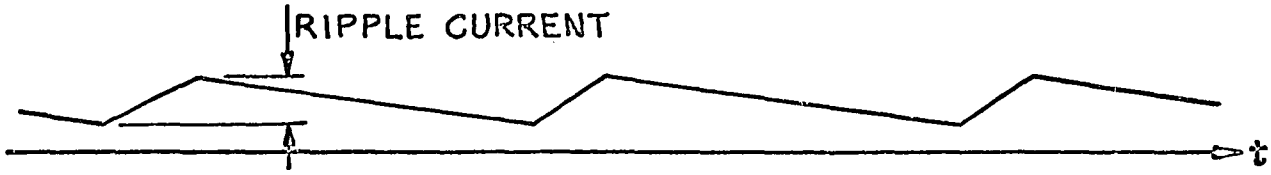
Consider separately periods 1 and 2, defined by equations (4) and (5) respectively.



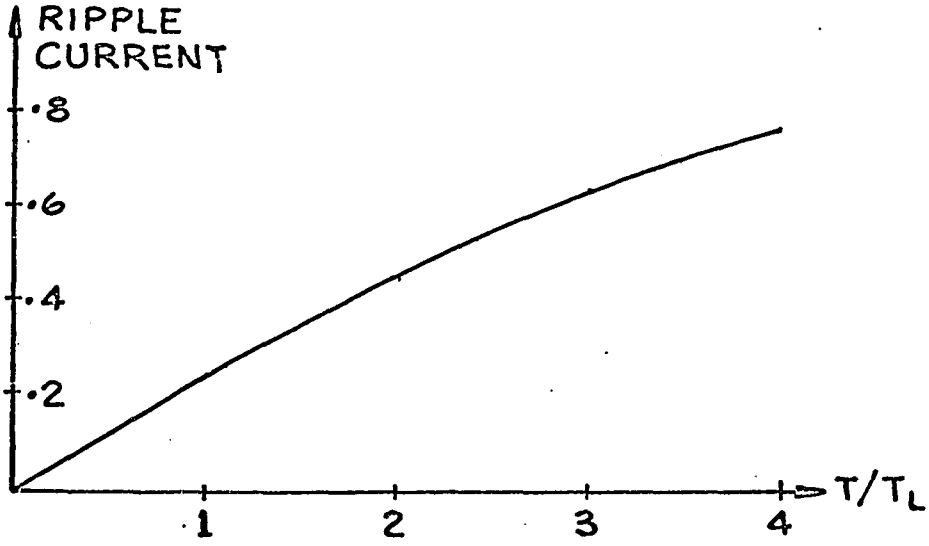
PWM: VOLTAGE-SOURCE EXCITATION



LOW-FREQUENCY EQUIVALENT OF THE LOAD



STEADY-STATE CURRENT IN INDUCTIVE LOADS



APP. 2.1 : PWM EXCITATION OF INDUCTIVE LOADS

<u>Period 1:</u> $mT < t < (m + b)T, \quad n = m - 1$

$$i(t) = 1 - Ae^{-gt} \tag{10}$$

$$A = \frac{e^{gmT}(e^{gT} - e^{gbT}) + e^{gbT} - 1}{e^{gT} - 1} \tag{11}$$

The steady state current is obtained by taking the limit of equation (10) as m tends to infinity,

$$\lim_{m \to \infty} i(t) = 1 - e^{-g(t - mT)} \frac{e^{gT} - e^{gbT}}{e^{gT} - 1} \tag{12}$$

It varies between the limits:

$$i(mT)_{ss} = 1 - \frac{e^{gT} - e^{gbT}}{e^{gT} - 1} \tag{13}$$

and

$$i(mT + bT)_{ss} = 1 - e^{-gbT} \frac{e^{gT} - e^{gbT}}{e^{gT} - 1} \tag{14}$$

The steady state ripple current is obtained by subtraction of equation (13) from (14), which yields:

$$i_{rss} = (1 - e^{-gbT}) \frac{e^{gT} - e^{gbT}}{e^{gT} - 1} \tag{15}$$

Differentiation of equation (15) with respect to "b" shows that the ripple attains a maximum at 50% duty cycle (b = 1/2), an intuitively obvious result. The value of i_{rss} at b = 1/2 reduces to the compact expression:

$$i_{r(b = 1/2)} = \tanh(gT/4) = \tanh(T/4T_1) \tag{16}$$

As expected, the ripple current is a function of the relative magnitudes of the load time-constant T_1 and the sampling frequency 1/T.

Figure Appendix II.1 shows that the ripple is equal to 5% of the average current when $T = 0.1T_1$.

To find an expression for the average current $\bar{i}(t)$, we must integrate equation (10) over period 1, and a corresponding equation over period 2. Let

$$Q1(t) = \int_{mT}^{(m + b)T} i(t)dt, \text{ then} \tag{17}$$

$$Q1(t) = bT - (A/g)(e^{-gmT} - e^{-g(m + b)T}) \tag{18}$$

<u>Period 2</u>: $(m + b)T < t < (m + 1)T \qquad n = m$

Substitution of the above conditions into equation (8) gives

$$i(t) = Be^{-gt} \tag{19}$$

where:

$$B = \frac{(e^{gbT} - 1)(e^{g(m + 1)T} - 1)}{e^{gT} - 1} \tag{20}$$

Let:

$$Q2(t) = \int_{(m + b)T}^{(m + 1)T} i(t)dt, \text{ then} \tag{21}$$

$$Q2(t) = (B/g)(e^{-g(m + b)T} - e^{-g(m + 1)T}) \tag{22}$$

We can now evaluate $\bar{i}(t)$ by addition of equations (18) and (22).

$$\bar{i}(t) = \frac{Q1(t) + Q2(t)}{T} \tag{23}$$

$$= b - e^{-gmT} \frac{(e^{gbT} - 1)(1 - e^{-gT})}{gT(e^{gT} - 1)} \tag{24}$$

The steady state value of $\bar{i}(t)$ is "b," as it would be with a purely resistive load.

The concept of the "time constant" creates some difficulties. Since the definition which is used in conjunction with step-excitation does not apply, we will define the effective time constant (t_{ef}) as the time required for $\bar{i}(t)$ to attain $1 - e^{-1}$ of its final value.

To evaluate t_{ef}, we divide the second element on the RHS of equation (24) by "b" and compare it to e^{-1}.

$$e^{-gmT} \frac{(e^{gbT} - 1)(1 - e^{-gT})}{bgT(e^{gT} - 1)} = e^{-1}, \text{ or} \tag{25}$$

$$t_{ef} = mT = (1/g) + (1/g)\ln. \frac{(e^{gbT} - 1)(1 - e^{-gT})}{bgT(e^{gT} - 1)} \tag{26}$$

For small values of gT, equation (26) simplifies to

$$t_{ef} = 1/g = L/R \tag{27}$$

the conventional time constant of the load impedance.

APPENDIX III

ACTIVE ANALOG RC FILTERS

Unlike their digital counterparts, analog filters are highly diversified. The configuration of analog networks varies not only with the order of the transfer-function, but also with the magnitude of its coefficients.

To arrive at a satisfactory realization, it is often necessary to synthesize a particular transfer-function by different procedures and to compare the merits of the resultant networks. While investigating the lack of commonalty in analog filters, we have discovered a new method of synthesis of active RC filters. We will present it here, although it appears to be out of context. It does illustrate the reasons for the diversity of analog implementations and it does present the derivation of the network which was used in the text of the thesis, for the purpose of comparison of analog and digital filters.

Let T(s) be the open-circuit voltage transfer function of a three-terminal, passive, RC network. Then,

$$T(s) = \frac{P(s)}{Q(s)} \tag{1}$$

where P(s) and Q(s) are polynomials in s. For reasons which will become apparent as the argument develops, rewrite equation (1) as

$$T(s) = \frac{P(s)}{P(s) + [Q(s) - P(s)]} \tag{2}$$

Let the passive network be connected to two ideal voltage-amplifiers, as shown in Figure 1. Denote the voltage at the output node of the passive network by V_o and observe that a voltage equal to kV_o is applied to the ground node of the passive network. Using the notation of Figure 1, formulate the following equations:

$$T(s) = \frac{P(s)}{Q(s)} = \frac{V_{21}'}{V_{11}'} = \frac{V_o - kV_o}{V_{in} - kV_o} \tag{3}$$

$$\frac{V_o}{V_{in}} = \frac{P(s)}{P(s) + (1 - k)(Q(s) - P(s))} \tag{4}$$

Equation (4) shows that the numerator of the transfer function T(s) is immune to ground node feedback. Except for a gain constant, the numerator of the transfer function of the active filter is the same as the numerator of the passive network.

To shed some light on the denominator of equation (4), let us turn to a few equations of network topology. The concepts of "trees" and two-trees" are defined in references S5 and S6. The open-circuit voltage transfer function of a two-port (Figure 2) is given by reference L6 as follows:

$$\frac{V_2}{V_1} = \frac{W_{12,1'2'} - W_{12',1'2}}{W_{1,1'}} \tag{5}$$

where:

$W_{ab,cd}$ = Sum of two-tree admittance products, nodes a and b in one part, c and d in the other.

Two subsidiary equations are necessary:

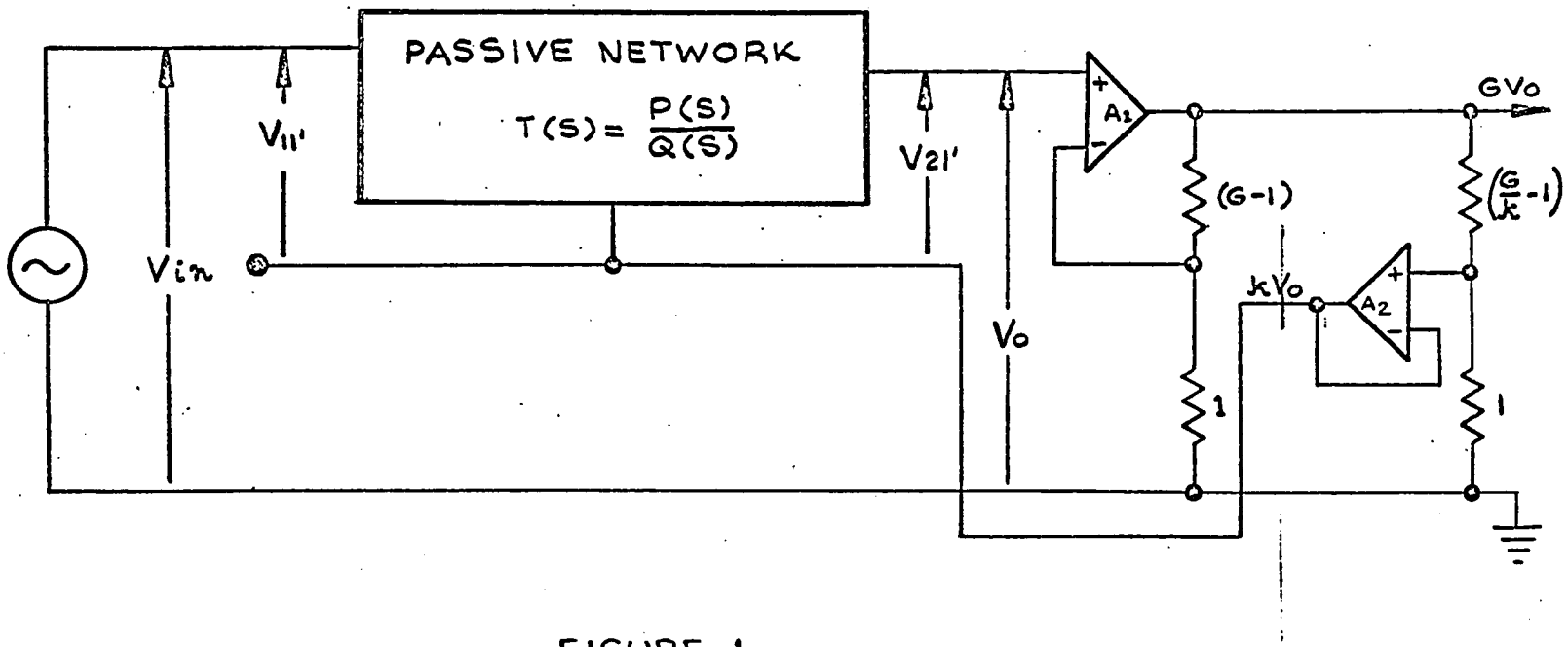
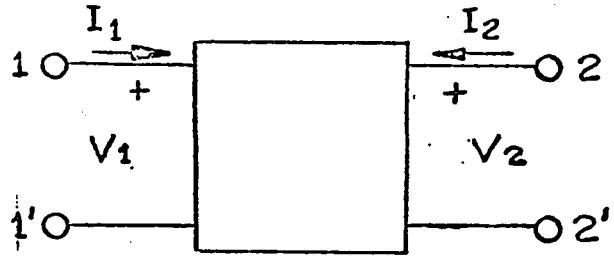
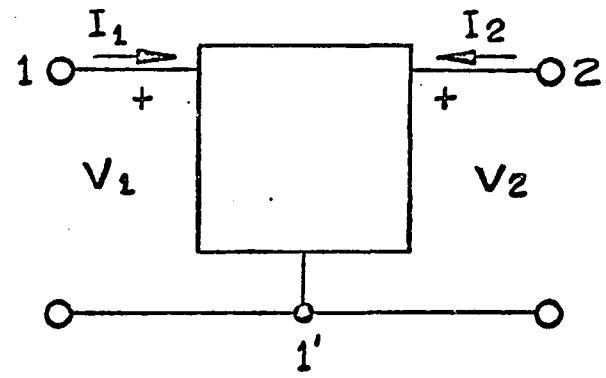


FIGURE 1

FEEDBACK TO THE GROUND NODE
OF A PASSIVE NETWORK



$$\frac{V_2}{V_1} = \frac{W_{12,1'2'} - W_{12',1'2}}{W_{1,1'}}$$



$$\frac{V_2}{V_1} = \frac{W_{12,1'}}{W_{1,1'}}$$

FIGURE 2
VOLTAGE TRANSFER FUNCTIONS OF TWO-PORTS AND THREE TERMINAL NETWORKS

$W_{a_1a_2\ldots a_n,\ b_1b_2\ldots b_m}$ = Sum of two-tree admittance products, nodes $a_1a_2\ldots a_n$ in one part, nodes $b_1b_2\ldots b_m$ in the other. (6)

$$W_{aa,cd} = W_{a,cd} \tag{7}$$

In a three terminal network, terminals 1' and 2' merge into a single terminal. Thus.

$$W_{12',\ 1'2} = W_{11',\ 1'2} = 0 \tag{8}$$

Furthermore, since

$$W_{a,cd} = W_{ab,cd} + W_{a,bcd} \quad \text{(if b belongs to the set acd)} \tag{9}$$

equation (5) degenerates to:

$$\frac{V_2}{V_1} = \frac{W_{12,1'}}{W_{1,1'}} = \frac{W_{12,1'}}{W_{12,1'} + W_{1,21'}} \tag{10}$$

Let us now stipulate that the polynomials P(s) and Q(s) be expressed in terms of admittance products, in order that we may compare equation (10) with equation (2) and make the following identifications:

$$P(s) = W_{12,1'} \tag{11}$$

$$Q(s) - P(s) = W_{1,21'} \tag{12}$$

Substitution of equations (11) and (12) into equation (4) leads to

$$\frac{V_o}{V_{in}} = \frac{W_{12,1'}}{W_{12,1'} + (1 - k)W_{1,21'}} \tag{13}$$

Equation (13) displays the desired result. It shows that two-trees $W_{1,21'}$ are susceptible to ground node feedback. Furthermore, since subsets $W_{12,1'}$ and $W_{1,21'}$ are mutually exclusive subsets, equation (13) shows also that two-trees $W_{12,1'}$ are immune to ground node feedback.

The application of the above conclusions to the analysis of filters whose configurations conform to Figure 1 is self-evident. Utilization of equation (13) in the synthesis of active RC filters will be demonstrated below.

Example.

Synthesize the transfer function $\theta(s)$,

$$\theta(s) = m \frac{k_2 s^2 + k_3 s + 1}{s^2 + k_1 s + 1} , \tag{14}$$

where: $0 < k_1 < 2$; $0 < k_2 < 1$; $0 < k_3 < 2(k_2)^{1/2}$

From past experience, or from tabulated data on passive RC filters (B1, B2) select a network which can produce the complex zero.

One candidate is shown in Figure 3. The numerator polynomial of this network is

$$W^*_{12,1'} = s^2 C_1 C_2 + s g_1 (C_1 + C_2) + g_1 g_2 \tag{15}$$

and the feedback-susceptible term of the denominator is

$$W^*_{1,21'} = s g_2 C_2 \tag{16}$$

Realization of the complex pole is predicated on the availability of a subset $W_{1,21'}$ with odd and even powers of s (recall $k_2 \neq 1$). It is therefore apparent that the desired transfer function cannot be realized by the network of Figure 3.

However, re-examination of equation (13) reveals an answer to the dilemma: the network must be modified by addition of components which change $W^*_{1,21'}$, but not $W^*_{12,1'}$. Multiplication of $W^*_{12,1'}$ by a constant is permissible.

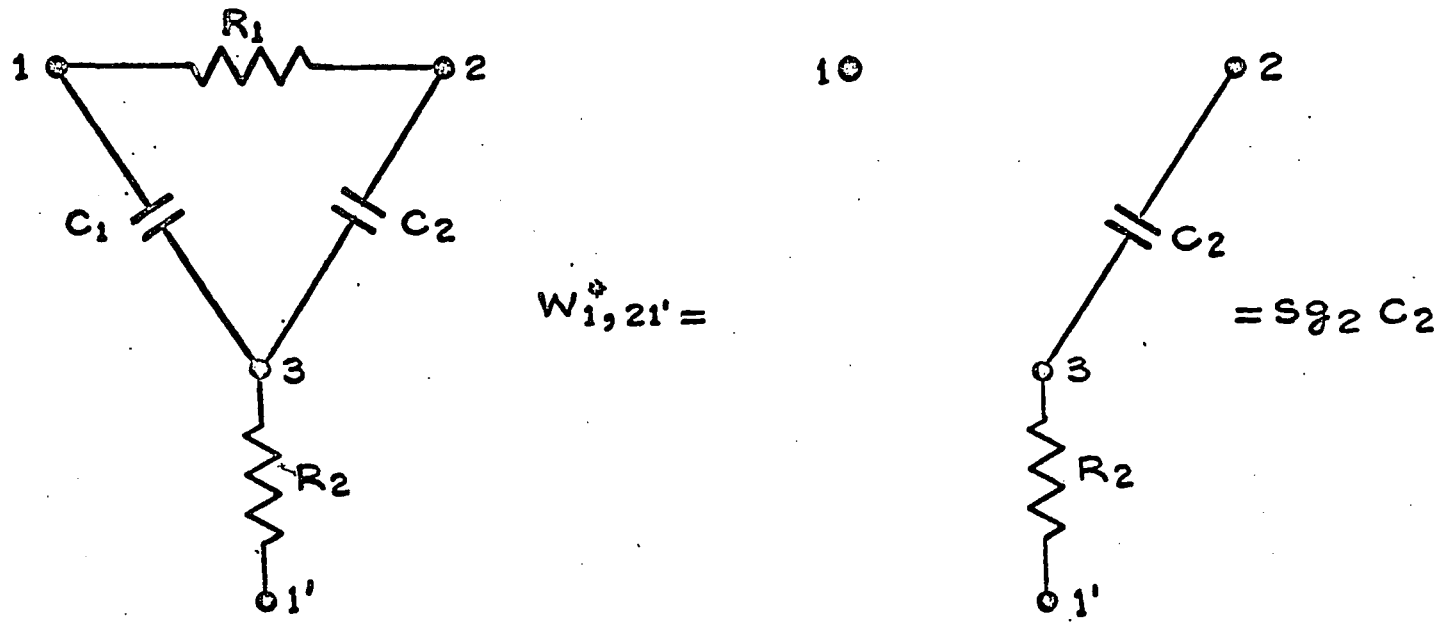


FIGURE 3
THE BASIC NETWORK

Figures 4 and 5 present two examples of such modifications. Both will realize the required transfer-function, at least for some values of the parameters k_i.

The limiting conditions are:

$$k_1 k_2 > k_3 \tag{17}$$

for Figure 4, and

$$k_2 + k_3(k_1 - k_3) > 1 \tag{18}$$

for Figure 5.

Equations (17) and (18) illustrate the restrictive nature of analog implementations. It is clearly impracticable to work with universal implementations, although one can develop better methods of synthesis of particular functions.

Figure 6 depicts a complete solution of the problem:

$$\theta(s) = 5\,\frac{(s/2000)^2 + (s/5000) + 1}{(s/1000)^2 + (s/1000) + 1} \tag{19}$$

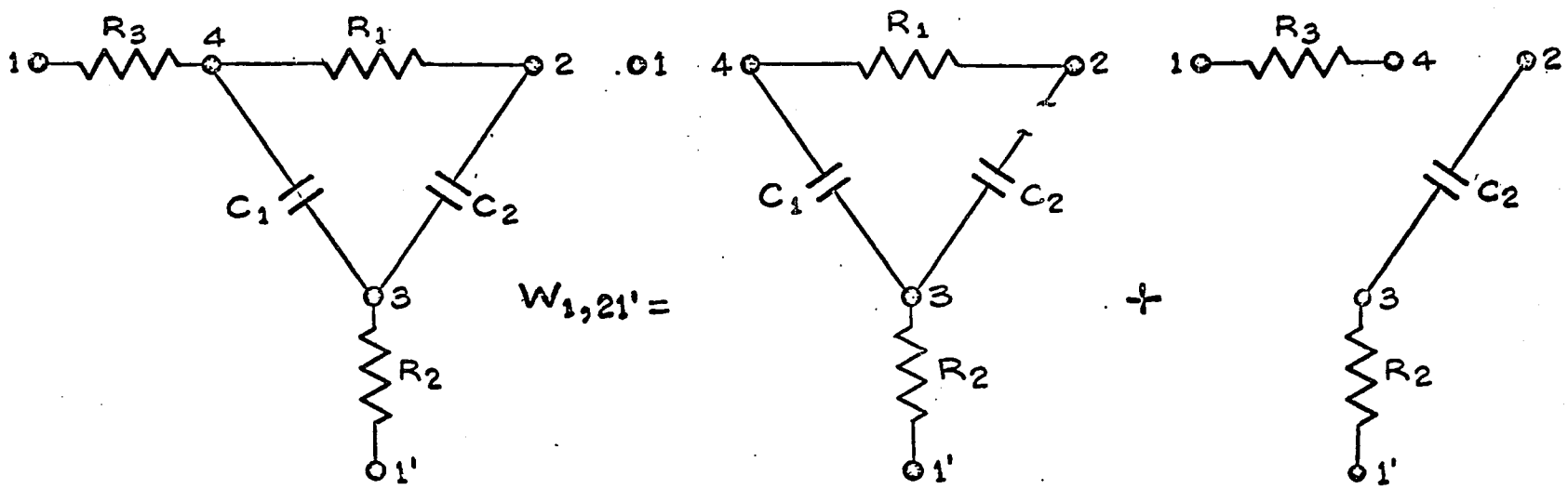


FIGURE 4

MODIFICATION NO. 1

$$W_{12,1'} = g_3 \, W^{*}_{12,1'}$$

$$W_{1,21'} = s^2 g_2 C_1 C_2 + s g_1 g_2 (C_1 + C_2) + s g_2 g_3 C_2$$

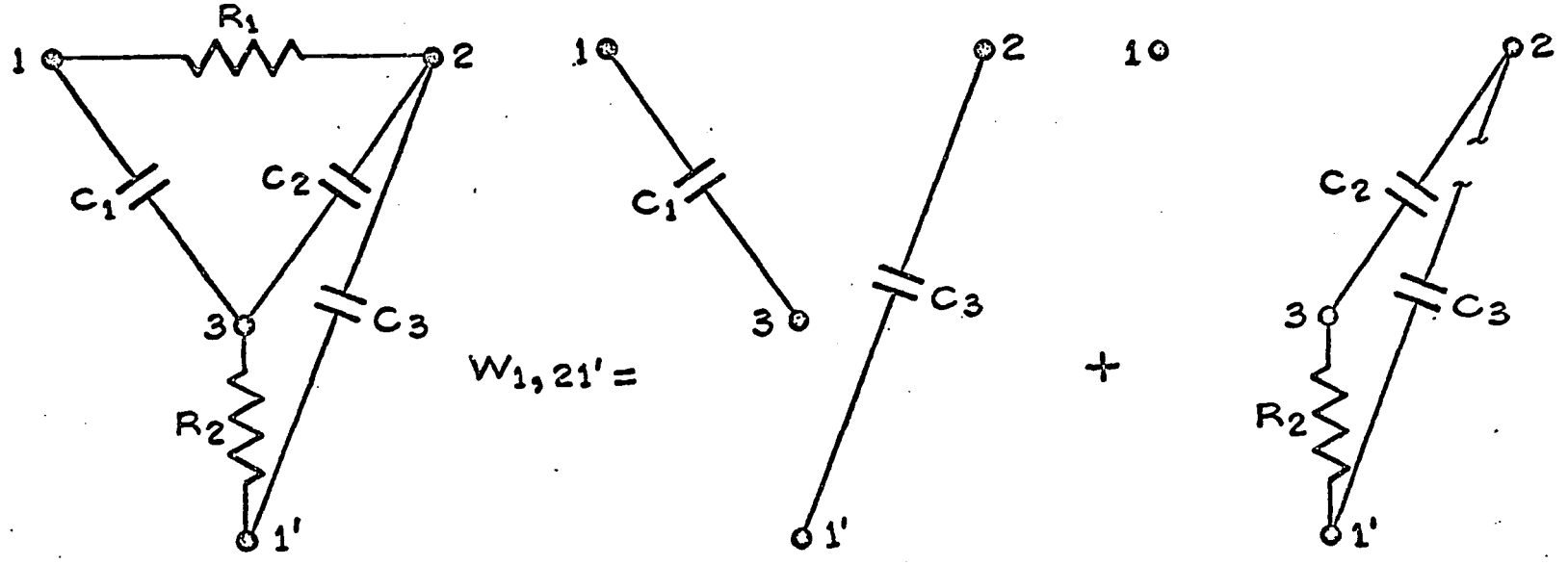


FIGURE 5

MODIFICATION NO. 2

$$W_{12,1'} = W^{*}_{12,1'}$$

$$W_{1,21'} = s^2 C_3 (C_1 + C_2) + s g_2 (C_2 + C_3)$$

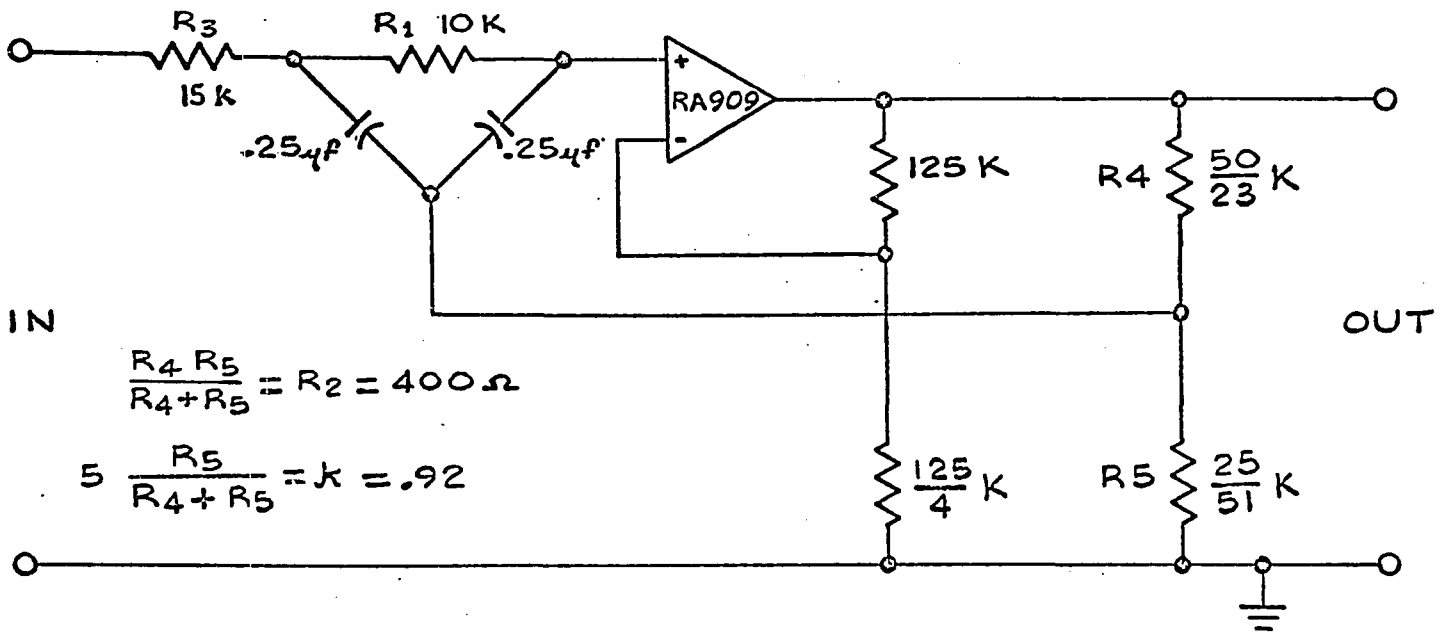


FIGURE 6

REALIZATION OF $\theta(S) = 5\,\dfrac{(S/2000)^2 + S/5000 + 1}{(S/1000)^2 + S/1000 + 1}$

REFERENCES

A1. Abate, J. E., "Linear and Adaptive Delta Modulation," Proc. IEEE, vol. 55, No. 3, March, 1967, pp. 298-308.

A2. Ahrons, R. W. and P. D. Gardner, "Open the Gate to Nanopower IC Logic," Electronic Design, vol. 19, September 13, 1967, pp. 81-87.

A3. Aseltine, J. A., Transform Methods in Linear System Analysis. New York: McGraw-Hill, 1958.

A4. Athans, M. and P. L. Falb, Optimal Control. New York: McGraw-Hill, 1966.

A5. Allison, J. F., F. R. Heiman and J. R. Burns, "Silicon on Sapphire Complementary MOS Memory Cell," IEEE Jour., Sol. State Circ., December, 1967, pp. 208-212.

B1. Balabanian, N. and I. Cinkilie, "Expansion of an Active Synthesis Technique," IEEE Trans. Circuit Theory, vol. CT. 10, June, 1963, pp. 290-299.

B2. Balabanian, N. and B. Patel, "Active Realization of Complex Zeros," IEEE Trans. Circuit Theory, vol. CT. 10, June, 1963, pp. 299-300.

B3. Bardeen, J. and W. H. Brattain, "Transistor, A Semiconductor Triode," Phys. Rev., vol. 74, 1948, pp. 230-231.

B4. Bellman, R. E., Dynamic Programming. Princeton, New Jersey: Princeton University Press, 1957.

B5. Bellman, R., Introduction to Matrix Analysis. New York: McGraw-Hill, 1960.

B6. Bellman, R. E. and S. E. Dreyfus, Applied Dynamic Programming. Princeton, New Jersey: Princeton University Press, 1960.

B7. Blackman, R. B., Data Smoothing and Prediction. Reading, Massachusetts: Addison-Wesley, 1965.

B8. Bode, H., Network Analysis and Feedback Amplifier Design. Princeton, New Jersey: D. Van Nostrand, 1945.

B9. Bogert, H. Z., "Metal Oxide Silicon Integrated Circuit Solid State Technology," IEEE Spectrum, March, 1966, pp. 30-35.

B10. De Boice, W. F., Integrated Circuit Design for a Low-Cost Inertial Guidance System, Defense Documentation Center, Technical Report No. AFAL-TR-65-18, February, 1965.

B11. Boysel, L., "Memory on a Chip: A Step Towards Large Scale Integration," Electronics, February 6, 1967, p. 92.

B12. Brigham, O. E. and R. E. Morrow, "The Fast Fourier Transform," IEEE Spectrum, December, 1967, pp. 63-70.

B13. Burger, R. M. and R. P. Donovan, Fundamentals of Silicon Integrated Device Technology. Englewood Cliffs, New Jersey: Prentice-Hall, 1967.

C1. Camenzind, H. R., "A Guide to Integrated-Circuit Technology," Electro-Technology, February, 1968, pp. 49-64.

C2. Camenzind, H. R., Circuit Design for Integrated Electronics. Reading, Massachusetts: Addison-Wesley, 1968.

C3. Cave, E. F. and B. R. Czorny, "Epitaxial Deposition of Silicon and Germanium Layers by Chloride Reduction," RCA Rev., vol. 24, December, 1963, pp. 523-545.

C4. Childers, D. G., "Study and Experimental Investigation of Sampling-Rate and Aliasing in Time-Division Telemetry Systems," IRE Trans. Space Electronics Telemetry, vol. SET 8, No. 4, December, 1962, pp. 267-283.

C5. Cho, Y. and F. G. Popp, A High-Speed Arithmetic Unit for Digital Filter Implementation, MIT, Lincoln Laboratory, MS-2024, October 26, 1967.

C6. Clausen, H. and R. B. Rusert, "Isolation Problems Get An Airing," Electronics, vol. 14, No. 9, April, 1968, pp. 75-78.

C7. Cooley, J. W. and J. W. Tukey, "An Algorithm for the Machine Calculation of Complex Fourier Series," Math. Comput., vol. 19, April, 1965, pp. 297-301.

C8. Chu, Y., Digital Computer Design Fundamentals. New York: McGraw-Hill, 1962.

D1. Deerfield, A., Canonical Digital Filters, NEREM 1967, Raytheon Co., Bedford, Massachusetts, November, 1967, pp. 1-11.

D2. Dickhaut, R. H., Comparison and Evaluation of Three Automated Circuit Analysis Programs, Defense Documentation Center, Report No. AD623 963.

D3. Dorf, R. C., Modern Control Systems. Reading, Massachusetts: Addison-Wesley, 1967.

E1. Evans, L., "Biasing FETs for Zero DC Drift," Electro Technology, August, 1964, p. 93.

F1. Fagin, S. L., "Feedback Realization of a Continuous-Time Optimal Filter," IEEE Trans. Aerospace and Electronic Systems, vol. AES-3, No. 3, May, 1967, pp. 494-509.

F2. Farina, D. E. and D. Trotter, "MOS Integrated Circuits Save Space and Money," Electronics, October 4, 1965, pp. 84-85.

F3. Flores, I., The Logic of Computer Arithmetic. Englewood Cliffs, New Jersey: Prentice-Hall, 1963.

F4. Freeman, H., Discrete-Time Systems. New York: John Wiley, 1965.

G1. Ghest, R. C., "Designing with IC Shift-Register Counters," The Electronic Engineer, April, 1968, pp. 49-53.

G2. Golomb, S. W., Digital Communications with Space Applications. Englewood Cliffs, New Jersey: Prentice-Hall, 1964.

G3. Grinich, V., R. Noyce and R. T. Kikoshima, Silicon Mesa Transistors For Use As Saturating Switches, Fairchild Semiconductor Corp., Report No. TP4.

G4. Goldman, S., Transform Calculus and Electrical Transients. Englewood Cliffs, New Jersey: Prentice-Hall, 1949.

H1. Happ, W. W., "Scope and Availability of Programs for Computer Aided Circuit Design," Solid-State Circuits Conference, February, 1967, Digest, pp. 64-65.

H2. Hill, F. H., A. S. Faber and H. N. Yu, "Silicon Versus Germanium in Picosecond Logic Circuits," ISSCC, 1967, pp. 112-113.

H3. Ho, Y. C., The Method of Least Squares and Optimal Filtering Method, Rand Corporation, Memorandum RM-3329-PR, October, 1962.

H4. Hoerni, J. A., Planar Silicon Transistors and Diodes, Fairchild Semiconductor Corp., Report No. TP14.

H5. Hoffait, A. H. and R. D. Thornton, "Limitations of Transistor DC Amplifiers," Proc. IEEE, vol. 52, February, 1964, pp. 179-184.

H6. Hsu, J. C. and A. U. Meyer, Modern Control Principles and Applications. New York: McGraw-Hill, 1968.

H7. Hurley, R. B., Transistor Logic Circuits. New York: John Wiley, 1961.

J1. Joseph, E. C., "Impact of Large Scale Integration on Aerospace Computers," IEEE Trans. Electronic Computers, vol. EC-16, No. 5, October, 1967, pp. 558-561.

J2. Jury, E. J., Sampled-Data Control Systems. New York: John Wiley, 1958.

K1. Kalman, R. E., New Methods and Results in Linear Prediction and Filtering, RIAS Technical Report, 61-1, 1961.

K2. Kalman, R. E., "Linear Stochastic Filtering Theory--Reappraisal and Outlook," Symposium on System Theory, Polytechnic Institute of Brooklyn, April, 1965, pp. 197-205.

K3. Kalman, R. E. and R. S. Bucy, "New Results in Linear Filtering and Prediction Theory," Journal of Basic Engineering, March, 1961, pp. 95-108.

K4. Karp, J., "Use Four-Phase MOS IC Logic," Electronic Design, April 1, 1967, pp. 62-67.

K5. Kret, D. B., D. Thompson and F. H. Bower, editors, "Epitaxial Growth in IC Fabrication," The Electronic Engineer, August, 1966, pp. 117-123.

K6. Kromer, H., "The Drift Transistor," Naturewissenschaften, vol. 40, November, 1953, pp. 578-579.

K7. Kuo, B. C., Analysis and Synthesis of Sampled-Data Control Systems. Englewood Cliffs, New Jersey: Prentice-Hall, 1963.

K8. Kuo, F. F., "Network Analysis by Digital Computer," Proc. IEEE, June, 1966, p. 820.

K9. Kuo, F. F. and J. Kaiser, editors, System Analysis by Digital Computer. New York: John Wiley, 1966.

L1. Lees, A. B., "Interpolation and Extrapolation of Sampled Data," IRE Trans. Inf. Theory, vol. IT2, 1956, pp. 12-17.

L2. Lee. Y. W., Statistical Theory of Communications. New York: John Wiley, 1963.

L3. Leith, F. A., High Energy Implantation of Materials, U. S. Gov. R & D Report, 10 July 1967, AD-652103.

L4. Lepselter, M. P., "Beam Lead Technology," Bell Sys. Tech. J., vol. 45, February, 1966, pp. 233-253.

L5. Levy, S. Y., R. J. Linhardt, H. S. Miller and R. D. Sidnam, "System Utilization of Large-Scale Integration," IEEE Trans. Electronic Computers, vol. EC-16, No. 5, October, 1967, pp. 562-566.

L6. Linden, D. A., "A Discussion of Sampling Theorems," Proc. IRE, vol. 47, No. 7, July, 1959, pp. 1219-1226.

L7. Lindorf, D. P., Theory of Sampled-Data Control Systems. New York: John Wiley, 1965.

L8. List, B. H., "Engineering Economy Problems of Integrated Circuits," IEEE International Convention Record, New York, March, 1968, p. 77.

L9. Lohman, R. D., "Applications of MOS FETs in Microelectronics," Solid State Technology, March, 1966, pp. 22-29.

L10. Lynn, D. K., C. S. Meyer and D. J. Hamilton, Analysis and Design of Integrated Circuits. New York: McGraw-Hill, 1967.

M1. MacDougall, J. S., Applications of the Silicon Planar II MOS FET, Fairchild Semiconductor Corp. Report APP-109, November, 1964, pp. 1-10.

M2. Madland, G. R. and J. Jolly, "The Importance of Integrated Circuits Yield to Engineers," The Electronic Engineer, August, 1966, pp. 88-92.

M3. Mantey, P. E., "State-Variable Selection for Efficient Computer Implementation of Linear Discrete Systems," Proc. Nat. Electronics Conf., vol. XXXIII, October, 1967, pp. 74-79.

M4. Mayorov, F. V., Electronic Digital Integrating Computers--Digital Differential Analyzers. New York: American Elsevier Publishing Company, 1964.

M5. Meyer, A. U., Pulse Frequency Modulation and Its Application in Feedback Systems. Evanston, Illinois: Northwestern University Press, August, 1961

M6. Miller, A. and H. Manasevit, "Single Crystal Cilicon Epitaxy on Foreign Substrates," Jour. Vacuum Sc. & Tech., vol. 3, March, 1966, pp. 68-78.

M7. Mitchel, M. M. and N. H. Ditrick, "Stability Effects in MOS Enhancement Transistors," Solid State Design, November, 1965.

M8. Moore, G. E., "Semiconductor Integrated Circuits," Microelectronics, E. Keonijan, editor. New York: McGraw-Hill, 1963.

M9. Monroe, A. J., Digital Processes for Sampled Data Systems. New York: John Wiley, 1962.

M10. Motorola Semiconductor Corp., MTTL iii, Advance Information Bulletin, 1968.

M11. Motorola Staff, "Catch the Wandering Threshold Voltage," Motorola Monitor, vol. 6, No. 2, 1968, pp. 18-21.

M12. Mulcahy, D. L., "What Aerospace Management Expects in Microcircuit Reliability," National Electronic Convention Record, Chicago, October, 1967, p. 754.

N1. Nichols, J. L., "A Logical Step for Read-Only Memories," Electronics, June 12, 1967, pp. 111-113.

N2. Noyce, R. N., "Making Integrated Electronics Technology Work," IEEE Spectrum, May, 1968, pp. 63-66.

P1. Padalino, J. J. and A. Tuszynski, "Note on the Analysis and Synthesis of Active RC Filters," IEEE Trans. Circuit Theory, vol. CT-15, no. 4, December, 1968.

P2. Panter, P. F., Modulation, Noise, and Spectral Analysis. New York: McGraw-Hill, 1965.

P3. Papoulis, A., Probability, Random Variables, and Stochastic Processes. New York: McGraw-Hill, 1965.

P4. Papoulis, A., The Fourier Integral. New York: McGraw-Hill, 1962.

P5. Petritz, R. L., "Current Status of Large Scale Integration Technology," IEEE Journal of Solid State Circuits, vol. SC2, No. 4, December, 1967, pp. 130-147.

P6. Phillips, A. B., Transistor Engineering. New York: McGraw-Hill, 1962.

P7. Pontryagin, L. W., V. G. Boltyanskii, R. V. Gamkrelidze and E. F. Mischenko, The Mathematical Theory of Optimal Processes. New York: John Wiley, 1962.

P8. Price, J. E., "Use an IC Counter Next Time," Electronic Design, April 12, 1966, pp. 62-66.

P9. Priel, U. and J. W. Hively, "An Integrated Current Mode Full Adder," ISSCC Digest, February, 1967, pp. 108-109.

R1. Rader, C. M. and B. Gold, "Digital Filter Design Techniques in the Frequency Domain," Proc. IEEE, vol. 55, No. 2, February, 1967, pp. 149-171.

R2. Ragazzini, J. R. and G. Franklin, Sampled-Data Control Systems. New York: McGraw-Hill, 1958.

R3. Ragonese, L. J., "A Circuit Design Approach for Enhancing the Yield of Complex Iterative Electronic Subsystems," Proc. IEEE, vol. 53, No. 12, December, 1964, pp. 1613-1616.

R4. Rapp, A. K., L. P. Wennick, H. Borkan and K. R. Keller, "Complementary-MOS Integrated Binary Counter," Solid State Circuits Conference, Philadelphia, Pennsylvania, 1967, pp. 52-53.

R5. Richman, J. and F. Thau, "Elements of the Kalman Filtering Technique," General Precision Technical News Bulletin, vol. 9, No. 3, 1966, pp. 13-18.

R6. Roberts, D. H., "Silicon Device Technology," IEEE Spectrum, February, 1968, pp. 101-108.

R7. Rowe, O. et al., "An Integrated Power Amplifier for the Saturn Vehicle Inertial Platform Gimbal Torquers," NEREM Record, November, 1966.

R8. De Russo, P. M., R. J. Roy and C. M. Close, State Variables for Engineers. New York: John Wiley, 1965.

S1. Schwartz, M., Information Transmission, Modulation and Noise. New York: McGraw-Hill, 1959.

S2. Schwartz, R. J. and B. Friedland, Linear Systems. New York: McGraw-Hill, 1965.

S3. Seeds, R. B., W. R. Smith and R. D. Nevala, "Integrated Complementary Transistor Nanosecond Logic," Proc. IEEE, vol. 52, No. 12, December, 1964, pp. 1584-1590.

S4. Serrell, R., "Elements of Boolean Algebra for the Study of Information-Handling Systems," Proc. IRE, vol. 41, No. 10, 1953, pp. 1366-1379.

S5. Seshu, S. and N. Balabanian, Linear Network Analysis. New York: John Wiley, 1959.

S6. Seshu, S. and M. B. Reed, Linear Graphs and Electrical Networks. Reading, Massachusetts: Addison-Wesley, 1961.

S7. Shanon, C. E., "Communications in the Presence of Noise," Proc. IRE, vol. 37, No. 1, January, 1949, pp. 10-21.

S8. Shileiko, A. V., Digital Differential Analysers. New York: The Macmillan Company, 1964.

S9. Shockley, W., Electrons and Holes in Semiconductors. Princeton, New Jersey: D. Van Nostrand Company, 1950.

S10. Shockley, W., "A Unipolar Field Effect Transistor," Proc. IRE, vol. 40, November 1952, pp. 1365-1376.

S11. Spenke, E., Elektronische Halbleiter. Berlin: Springer-Verlag, 1956.

S12. Swerling, P., "First Order Error Propagation in a Stagewise Smoothing Procedure," The Journal for Astronautical Sciences, vol. 3, No. 6, 1959, pp. 46-52.

T1. Talley, J. R., "An Integrated Sense Amplifier," Proc. National Electronics Conference, Chicago, October, 1967, pp. 325-329.

T2. Texas Instruments, Type SN7500 Monolithic Silicon Sense Amplifier, New-Product Bulletin, Dallas, Texas.

T3. Tomovic, R., Introduction to Nonlinear Automatic Control Systems. New York: John Wiley, 1966.

T4. Tompkins, J. D., "FET Terminology and Parameters," Electrical Design News, July 1964, p. 48.

T5. Torng, H. C., Introduction to the Logical Design of Switching Circuits. Reading, Massachusetts: Addison-Wesley, 1964.

T6. Tou, J. T., Optimum Design of Digital Control Systems. New York: Academic Press, 1963.

T7. Troxel, D. I., "Reliability Techniques Application--Military Systems," IEEE International Convention Record, March, 1968, p. 153.

T8. Tuszynski, A., "Correlation Between the Base-Emitter Voltage and its Temperature Coefficient," Solid State Design, July, 1962, pp. 32-35.

T9. Tuszynski, A., "Skirting Thin-Film Design Problems," Microelectronics Design, H. Bierman, editor. New York: Hayden Co., 1966, pp. 79-85.

V1. Valdes, L. B., The Physical Theory of Transistors. New York: McGraw-Hill, 1961.

V2. Van Der Ziel, A. and J. W. Ero, "Small Signal, High-Frequency Theory of Field Effect Transistors," IEEE Trans. Electron Devices, vol. ED-11, No. 4, April, 1964, pp. 125-135.

V3. Van Hoorde, G. R., "Evaluation and Experience with Microelectronic Integrated Circuits," National Electronic Conference Record, Chicago, October, 1967, pp. 754-755.

W1. Warner, M., editor, Integrated Circuits. New York: McGraw-Hill, 1965.

W2. Warner, R. M., "Comparing MOS and Bipolar Integrated Circuits," IEEE Spectrum, June, 1967, pp. 50-58.

W3. Watt, C. W., "Reliability Achievement for Microelectronic Devices," IEEE International Convention Record, New York, March, 1968, p. 77.

W4. Wegener, H. A. R., "Silicon Nitride and Silicon Oxide in Insulated-Gate Field Effect Transistors," NEREM Record, 1966.

W5. Weimer, P. K., "The TFT, A New Thin Film Transistor," Proc. IRE, vol. 50, June, 1962, pp. 1462-1469.

W6. Wiener, N., Extrapolation, Interpretation and Smoothing of Stationary Time Series. New York: John Wiley, 1949.

W7. Weiss, "Monolithic Sub-Nanosecond Switch," ISSCC, 1966, pp. 8-9.

W8. White, H. V. and H. R. Carley, A Switching Mode Servo Amplifier Using Pulse Width Modulation, U. S. Army Missile Command, Report No. RG.TR-65-5, April, 1965.

W9. Widlar, R. J., Drift Compensation Techniques for Integrated DC Amplifiers, National Semiconductor Corp., Publication AN-3, 1964.

W10. Widlar, R. J., A High Speed Differential Comparator, Fairchild Semiconductor Corp., March, 1965.

W11. Widlar, R. J., "Some Circuit Design Techniques for Linear Integrated Circuits," IEEE Trans. Circ. Theory, vol. 12, December, 1965, pp. 586-590.

Y1. Yen, Y. T., "Transient Analysis of Four-Phase MOS Switching Circuits," IEEE J. Solid State Circuits, vol. 3, No. 1, March, 1968, pp. 1-5.

Z1. Zadeh, L. A. and C. A. Desoer, Linear System Theory. New York: McGraw-Hill, 1963.

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